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RF magnetron triode sputtering of CdTe and ZnTe films and solar cells

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RF magnetron triode sputtering of CdTe and ZnTe films and solar cells

by

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has met the dissertation requirements of Iowa State University

Signature was redacted for privacy.

Major Professor

Signature was redacted for privacy.

For the Major Program

To my wonderful wife,
Inga

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ABSTRACT

The n-CdS/p-CdTe solar cell has been researched for many years now. Research groups use a variety of processes to fabricate thin-film CdS/CdTe cells, including physical vapor deposition, chemical vapor deposition, and RF diode sputtering. One of the central areas of investigation concerning CdS/CdTe cells is the problem of a Schottky barrier at the back contact. Even cells fabricated with ohmic back contacts degrade into Schottky barriers as the devices are used. This severely degrades power generation. One possible solution is to use p^+-ZnTe as an interlayer between CdTe and the back contact. ZnTe is easily doped with Cu to be p-type. However, even contacts with this ZnTe interlayer degrade over time, because Cu is highly mobile and diffuses away from the contact towards the CdS/CdTe junction. Another possibility is to dope ZnTe with N. It has been demonstrated using molecular beam epitaxy and RF diode sputtering.

In this study, CdTe films are fabricated using a variation of RF diode sputtering called triode sputtering. This technique allows for control of ion bombardment to the substrate during deposition. Also, a higher plasma density near the target is achieved allowing depositions at lower pressures. These films are characterized structurally to show the effects of the various deposition parameters.

N-doped ZnTe films are also fabricated using this technique. These films are characterized electrically to show the effects of the various deposition parameters. Also, the effects of post-deposition annealing are observed. It is found that annealing at the right temperature can increase the conductivity of the films by a factor of 3 or more. However, annealing at higher temperatures decreases the conductivity to as low as 12% of the initial conductivity.

Finally, RF triode sputtered N-doped ZnTe films are used as an interlayer at the back contact of a CdS/CdTe solar cell. The effects of annealing the device before and after contact deposition are observed. Annealing before depositing contacts results in an increase in V_{oc} of 20mV. Annealing after contact deposition results in a degradation of fill factor over time.

CHAPTER 1: INTRODUCTION

1.1 Research and Commercial Potential

CdTe is a leading material for solar cell technology because of its nearly ideal direct bandgap (1.5eV) for absorption of solar energy, and because of the low cost and adaptability to large-scale manufacturing.[1] In particular, thin-film CdS/CdTe heterojunction cells are being investigated by several groups in a lab setting using various deposition techniques.[2-9] Manufacturing of commercial solar modules is now under way by a small number of companies in the U.S. and abroad[1] (Matsushita; Global Solar Energy, LLC; Golden Photon, Inc.; and Solar Cells, Inc., to name a few). To date, the highest cell efficiencies reported in the lab are near 16%. Champion module efficiencies of 9.1% have been realized for commercial production.[1]

1.2 Basic CdS/CdTe Structure

The typical CdS/CdTe cell structure is shown in Figure 1. A transparent conductive oxide (TCO) such as SnO_2 or indium tin oxide (ITO), which acts as the front contact, is applied to a glass superstrate. Next is a thin (100-500nm), highly doped, n-type CdS layer. CdS has a bandgap energy of 2.4eV, letting most of the light pass through to the relatively thick (2-5μm), lightly doped, p-type CdTe absorbing layer. This CdTe must be annealed at ~500°C in order to get a device-quality film. It is usually annealed in air or some other O_2-containing ambient, where the O_2 dopes the CdTe film to be slightly p-type. A Cu alloy or graphite paste is used as the back contact.

An energy band diagram of an ideal CdS/CdTe cell (with ohmic contacts, no defects, etc.) at 0 bias is shown in Figure 2. Again, light passes through the CdS layer to the CdTe, where the photons are absorbed and electron-hole pairs are created. Any electrons generated within a diffusion length of the depletion region are collected, thus creating current flow. Since the conduction bands of CdTe and CdS line up closely, there is nothing to block electron flow from CdTe to CdS. Most of the bandgap difference is in the valence band, which provides a large barrier to prevent holes from flowing back towards the TCO contact.

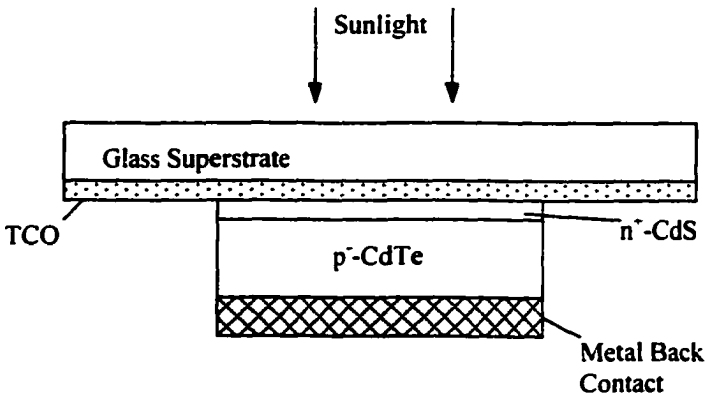

Figure 1: CdS/CdTe superstrate structure.

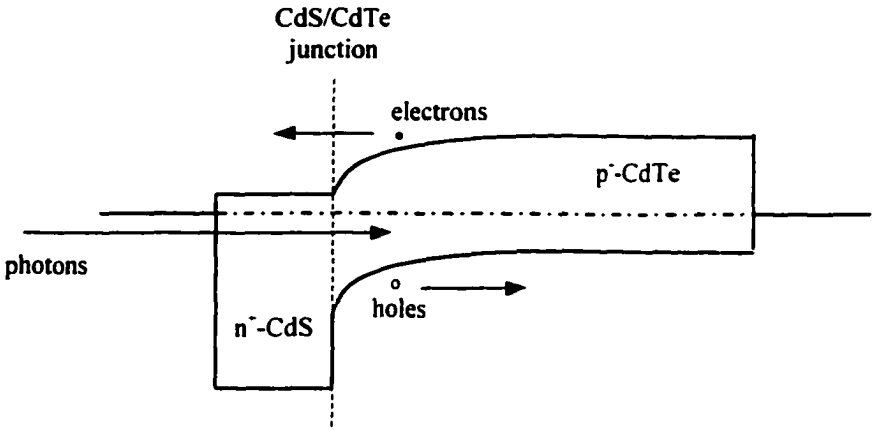

Figure 2: CdS/CdTe band diagram.

CHAPTER 2: CURRENT RESEARCH EFFORTS

2.1 The CdS/CdTe Junction

2.1.1 JUNCTION PROBLEMS

There are two primary areas currently under investigation in the literature. The first is the CdS/CdTe junction interface itself. As previously mentioned, after the CdS and CdTe layers are deposited, an anneal step is necessary to make CdTe a device-quality film. Not only does this step dope CdTe with oxygen to be slightly p-type, but it also increases the size of the grains by an order of magnitude or more. This leads to fewer defects, increased absorption, less recombination, and higher carrier mobility within the CdTe film. However, this step also has the effect of promoting diffusion of S into the CdTe layer and Te into the CdS, thus introducing many defects at the CdS/CdTe junction, increasing recombination there, and reducing shunt resistance. Another concern of the junction is the lattice mismatch of the two layers. The lattice constants of CdTe (6.48Å) and CdS (5.83Å) are dissimilar enough to cause considerable strain near the junction, again introducing defects. It is thought, however, that the anneal step may actually relax this strain.[4]

2.1.2 $CdCl_2$ TREATMENTS

2.1.2.1 Methanol Method

The issues described in the previous section are dealt with by performing the anneal step in the presence of $CdCl_2$.[11] Typically, a saturated solution of $CdCl_2$ in methanol is applied to the CdTe film with an eye dropper or spray bottle, or by dipping the CdTe into the solution for a short time. The methanol is allowed to evaporate, leaving a film of $CdCl_2$ behind. The sample is then put into a furnace where it is annealed for 30min to 2hr, depending on film thickness, temperature, etc. After the anneal, the $CdCl_2$ is rinsed off the CdTe. The result is actually a better-quality film (i.e., larger grains) than without $CdCl_2$, as well as increased O-doping of the film. Apparently, $CdCl_2$ acts as an activation-energy-lowering agent, which enables the anneal with $CdCl_2$ to be done at a lower temperature than without $CdCl_2$. This means there is less S and Te diffusion at the junction. The $CdCl_2$ treatment is sometimes performed on the CdS layer as well as the CdTe.[3] This further

reduces the S diffusion, since the S is bound in larger, more stable grains before the CdTe is deposited and annealed.

This method of $CdCl_2$ heat treatment, however, has several problems.[11] It is difficult to get a uniform coating of $CdCl_2$ across the CdTe film if the methanol is not allowed to evaporate evenly. Also, if the air above the evaporating methanol has a high humidity, localized clumping (even microscopic clumping) of the $CdCl_2$ occurs, resulting in small $CdCl_2$ cones. Even if the coating is even across the surface, the $CdCl_2$ thickness itself is difficult to control. Finally, when the $CdCl_2$ is rinsed away after the anneal, a Cl residue is left behind.

2.1.2.2 LPVD Method

A couple of research efforts have come up with alternatives to the $CdCl_2$/methanol treatment. Compaan applies $CdCl_2$ by laser physical vapor deposition (LPVD).[2] This method is performed under vacuum. A target of $CdCl_2$ is hit with an excimer laser, vaporizing material from the target to be deposited on the sample above it. The angle of the laser and target are controlled in such a way as to distribute the material evenly across the sample, with no clumping. The thickness of the $CdCl_2$ is easily controlled with deposition time. This method, however, still involves applying $CdCl_2$ directly onto the CdTe surface. Thus, after the anneal and rinse, Cl residue likely remains on the CdTe film.

2.1.2.3 $CdCl_2$ Vapor Method

McCandless does not apply $CdCl_2$ directly onto the CdTe surface.[3,11] Instead, the CdTe is annealed in the presence of both oxygen and $CdCl_2$ vapor. A description of the process is given in a later section. Since the $CdCl_2$ passes over the CdTe as a vapor, the film is annealed evenly and consistently. The amount of anneal and the amount of $CdCl_2$ reacting with the film is easily controlled by increasing or decreasing the total pressure of the Ar and O_2. Because the $CdCl_2$ is not directly deposited onto the CdTe film in solid form, there is no $CdCl_2$ to be rinsed off after the anneal. Finally, because the $CdCl_2$ is in vapor form, any unreacted Cl_2 gas flows away from the CdTe film during the anneal. Thus, there is no Cl residue left on the film.

2.2 CdTe Back Contact

The second primary area of concern in the literature with CdS/CdTe solar cells is the back contact to CdTe. Most metals form large Schottky barriers with p-type CdTe, resulting in high contact resistance and, thus, high series resistance in the cell.[12] Figure 3 gives an illustration of typical I-V curves of a solar cell with an ohmic back contact and a Schottky barrier at the back contact. A discussion of a typical I-V curve of a solar cell is presented in a later section. Notice how the Schottky barrier creates a double diode and reduces the fill factor of the I-V curve. Also notice the increase in series resistance with the Schottky barrier.

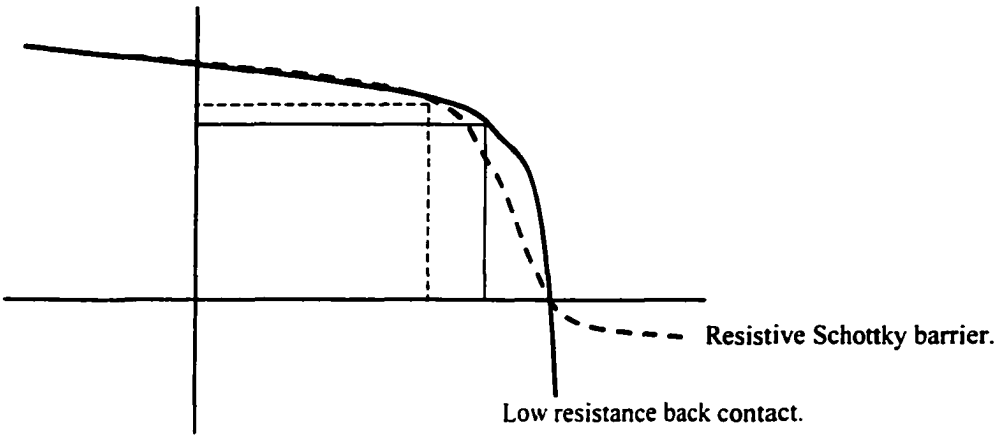

Figure 3: I-V curves for low resistance (ohmic) and Schottky barrier back contacts with corresponding fill factors.

2.2.1 ETCHING AND DOPING CdTe

A possible solution to the back contact problem is to create a tunnel junction by doping CdTe to be heavily p-type. As it turns out, it is quite difficult to incorporate p-type dopants into CdTe in high densities. McCandless has developed a method of contacting to CdTe involving a series of surface etchings and deposition of a thin layer of Cu to highly dope the surface of CdTe before applying a carbon ink conductor as the back contact.[10] The etching steps have two main purposes. First, the native CdO layer is etched away. Second, the surface of the film and the surfaces of the grains are left Te-rich, which makes the CdTe

highly p-type. The result of this procedure is a layer of Cu_xTe at the CdTe/carbon ink junction. The barrier height of this contact was measured to be 0.3eV.

2.2.2 p^+-ZnTe AS AN INTERLAYER AT THE BACK CONTACT

Another possible method of creating an efficient contact is to deposit a semiconductor with a small valence band discontinuity with CdTe and which can be doped to be highly p-type in order to create a tunnel barrier. ZnTe doped with Cu is one such semiconductor. Figure 4 shows two band diagrams of the back contact, with and without the ZnTe:Cu layer. Gessert,[12] Compaan,[13] and others have been working with p^+-ZnTe:Cu and have successfully made contact to CdTe. These methods still involve etching procedures to remove native CdO layers.

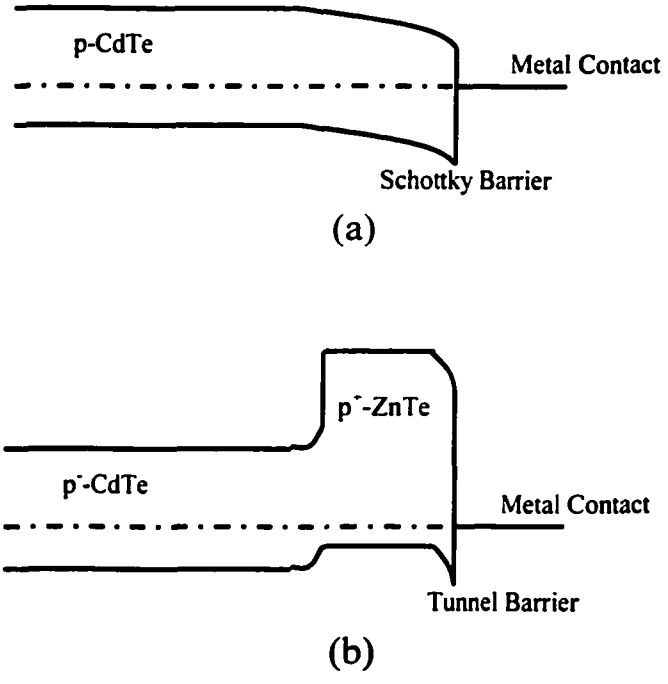

Figure 4: CdTe back contact (a) without and (b) with p^+-ZnTe interlayer.

2.2.3 DIFFICULTIES WITH ETCHING AND ZnTe

There are two main problems with these contacting procedures. First, the etching procedures are wet chemical etches. Wet chemical etching processes are more difficult to

transfer from the lab to commercial manufacturing, because they limit throughput. Gessert, on the other hand, has developed an all-dry etching process involving ion beam exposure followed by ZnTe:Cu deposition.[12]

Second, diffusion of Cu (whether it is pure Cu or Cu found in the ZnTe layer) into the CdTe layer is difficult to control.[4] Although Cu is a p-type dopant for CdTe and, thus, beneficial for lowering series resistance, if Cu is allowed to diffuse far enough, it will create defects in the absorbing layer and reduce lifetime. It may also affect the CdS/CdTe junction.

2.3 CdS/CdTe Substrate Configuration

Singh is working with CdS/CdTe cells in a substrate configuration,[4] as shown in Figure 5. In this case, Singh uses Mo foil as the substrate. Before depositing CdTe, thin layers each of Cu and Te are deposited to make a low-resistance contact to the CdTe. Since the contact surface of CdTe is never exposed to air, no etch is necessary (nor is an etch possible) to get rid of CdO. The CdTe film is heat treated with $CdCl_2$ by way of the methanol treatment previously described. CdS is then deposited and $CdCl_2$ annealed, followed by an ITO front contact layer. Although Singh has only achieved 5.3% efficiency due to a low shunt resistance, a V_{oc} of 824mV was obtained. This can be compared to a record V_{oc} of ~850mV for the glass superstrate configuration.

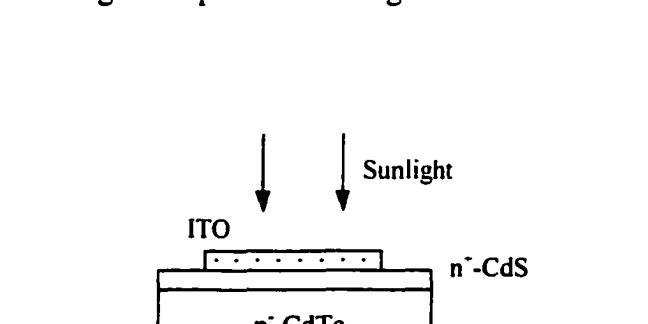

Figure 5: CdS/CdTe substrate solar cell.

The substrate configuration has a few advantages. One advantage is the use of the flexible metal substrate, which is more easily adaptable to commercial production than a glass substrate. Another advantage is that the thicker CdTe layer is deposited and a long $CdCl_2$ anneal is performed before the much thinner CdS layer and short $CdCl_2$ anneal. The ability to do a short anneal (if at all) when the CdTe and CdS layers are in contact with each other leads to less diffusion of S and Te at the junction. Also, the $CdCl_2$ can have a larger effect on the junction. There is a smaller layer through which $CdCl_2$ must diffuse, in order to get to and react with the junction to passivate defects, etc.

2.4 ZnTe Films Doped With N

Compaan has successfully deposited p-type ZnTe films doped with N using reactive sputtering.[13] Reactive sputtering is simply sputtering in the presence of a reactive gas. For example, a possible technique for depositing SiO_2 is to sputter Si in the presence of O_2 gas. A pure Si target is used for the sputtering material, while the ambient used is a mixture of O_2 and Ar. Instead of co-sputtering ZnTe and Cu, a pure ZnTe target is used. The sputtering ambient, instead of pure Ar, is a mixture of ~5%N_2/95%Ar. Compaan has achieved conductivities of ~0.1/Ωcm, with activation energies of 90meV.[13]

2.5 Triode Sputtering

Diode and triode sputtering are described in a later section. In short, triode sputtering incorporates a grounded (or biased) metal mesh between the target and substrate, thus moving the ground plane away from the substrate. The plasma is kept away from the substrate as well. Ion bombardment of the substrate can then be controlled with a negative DC bias without affecting the plasma. Fontana and Muzart[14], studying DC triode sputter deposition of titanium thin films, reported that because ionization rates were higher with the triode configuration than with a diode configuration, much lower deposition pressures were possible. This resulted in higher film densities.

Although many research groups have performed DC triode sputtering with many different metals, it appears that no one has attempted to employ this technique with semiconductor materials.

CHAPTER 3: RESEARCH OBJECTIVES

In light of the current state of research, the goals of this project are as follows:

1. Deposit CdTe films with the triode sputtering technique using varying deposition parameters. The films will be characterized structurally by various methods to be described in a later section.

2. Fabricate and characterize CdS/CdTe solar cells in a substrate configuration on Mo-foil. The triode sputtering technique will again be used for the CdTe layer. Cell data will be correlated to CdTe film data from goal 1.

3. Deposit N-doped ZnTe films using the triode sputtering technique to reactively sputter in a N_2 ambient. These films will be characterized electrically by various methods to be described in a later section, and the data will be compared to previous work, especially Compaan.[13]

4. Fabricate and characterize CdS/CdTe solar cells using N-doped ZnTe at the back contact. Cell data will be correlated with ZnTe film data from goal 3.

This work represents the first known effort to utilize triode sputtering to deposit semiconductor materials. It is believed that triode sputtering will allow better control of ion bombardment to the substrate.

Also, this is the second known effort to reactively sputter ZnTe in a N_2 ambient, and the first to use N-doped ZnTe at the back contact. As mentioned before, Cu-doped ZnTe is sometimes used as a back contact interlayer in CdS/CdTe solar cells. This layer usually consists of about 6% Cu. The Cu can diffuse into the CdTe layer as far as the CdS/CdTe junction. When the Cu diffuses out of the ZnTe layer, not only does the conductivity of the ZnTe layer degrade, defects are also created in the CdTe layer. If N can instead be used as the dopant for the ZnTe layer, this will eliminate Cu diffusion into the CdTe layer.

CHAPTER 4: MATERIAL AND DEVICE FABRICATION

4.1 RF Magnetron Sputtering

4.1.1 DIODE SPUTTERING

The process of sputtering is depicted in Figure 6. Two electrodes A and B are in a vacuum chamber at pressures in the 1-50mTorr, depending on the specific process. Electrode A acts as the anode and holds the substrate on which the film is to be deposited. The temperature of the substrate may be varied. Electrode B is the cathode and holds the material to be deposited, which is in the form of a "target." In this study, the target is a 3" diameter pressed powder disc. The ambient is usually an inert gas such as Ar (Ar is used for this study).

A negative bias is applied with RF power to the cathode (target) while the anode (substrate) is usually held at ground or allowed to float. (The walls of the sputtering chamber are always grounded.) The applied negative bias creates an electric field which accelerates electrons in the gas away from the target. When these electrons collide with Ar atoms, there are two possible outcomes. The colliding electron may excite an electron in the Ar atom to a higher energy level. The excited electron will then relax and emit a photon, creating the characteristic glow of the plasma. The other possible outcome is that an electron could be stripped from the Ar atom altogether. The resulting Ar^+ ion is then accelerated in the electric field toward the target, bombarding the target and ejecting material from the surface (hence the name, "target"). The ejected material may go in any direction to be deposited on any surface in the chamber. The surface of interest, of course, is the substrate.

In magnetron sputtering, the plasma is confined just over the target by a magnetic field created by magnets placed under the cathode as in Figure 7. This figure shows a top view and a cross section of the magnets with field lines. As electrons are accelerated away from the cathode by the electric field, the magnetic field lines direct the electrons back towards the target by the well-known equation

$$\mathbf{F} = e(\mathbf{v} \times \mathbf{B} + \mathbf{E}),$$

thus confining the plasma. The annular configuration of the magnets creates a magnetic field which causes the sputtering to occur in a ring as shown by the eroded area in Figure 7.

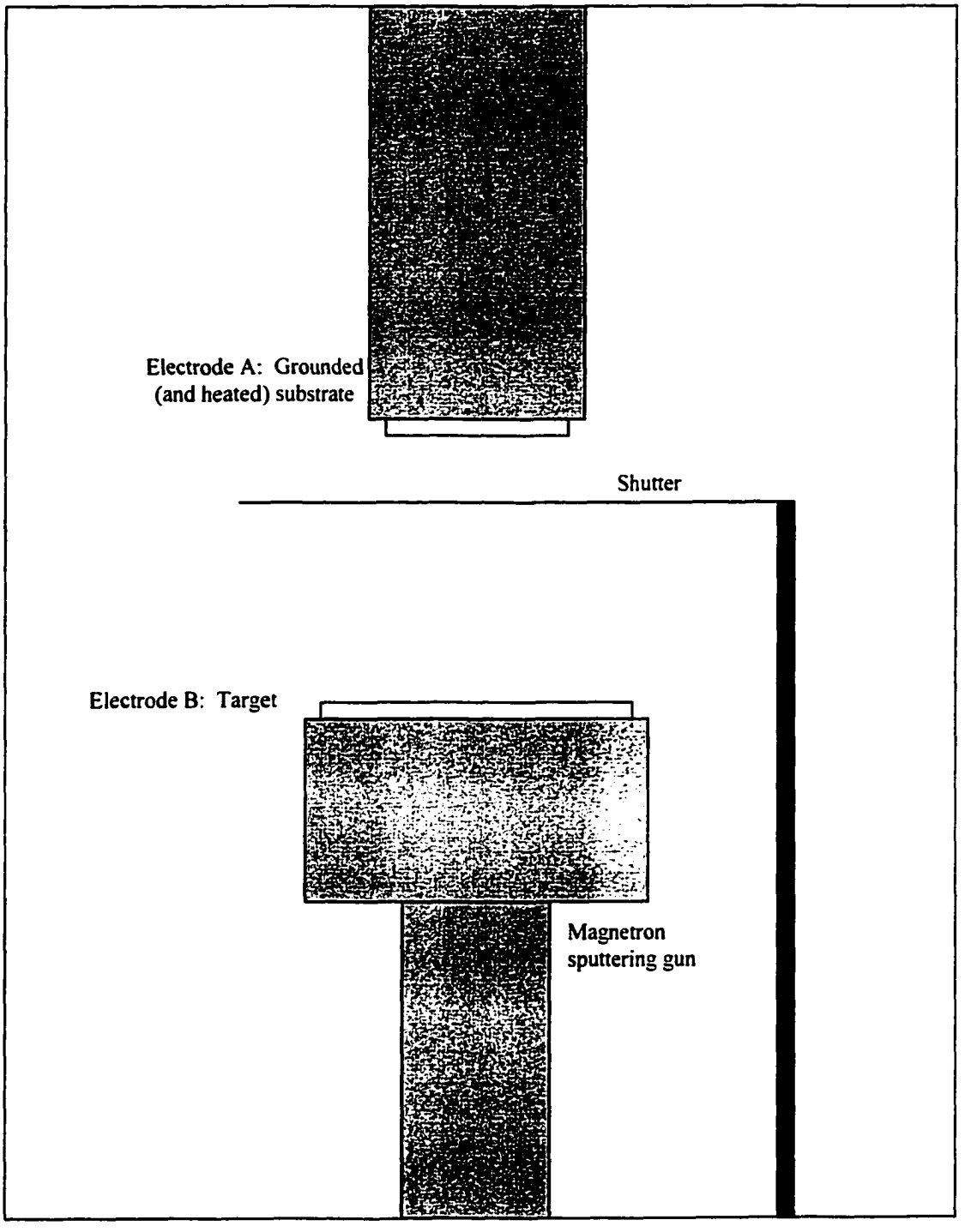

Figure 6: Schematic of diode sputtering system.

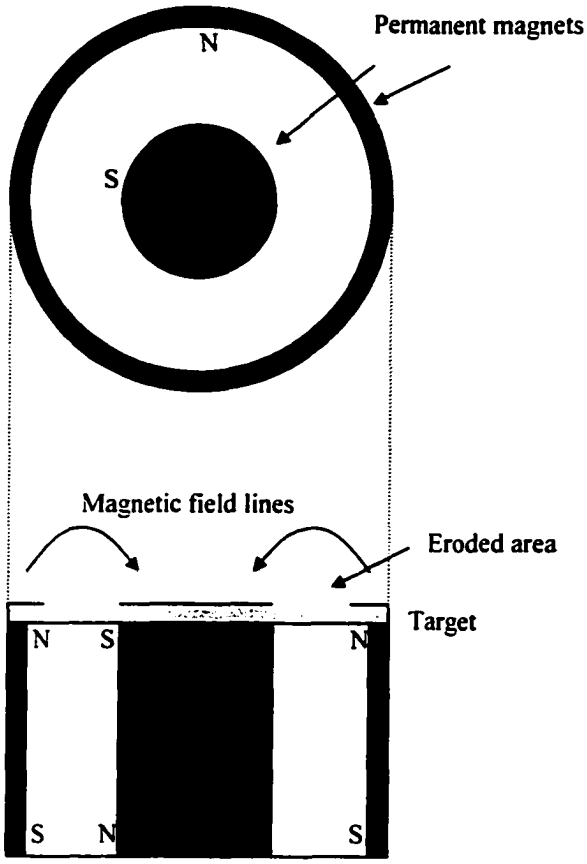

Figure 7: Magnet configuration of magnetron sputtering gun.

4.1.2 EFFECTS OF SPUTTERING PARAMETERS

Film properties are determined in part by the following deposition parameters: substrate temperature, ambient pressure, sputtering power, and target-substrate distance. Ultimately, these parameters contribute to the velocity of the deposited material at the substrate surface (known as surface velocity), the etching of or damage to the film from ion bombardment and material impact, and the deposition rate.

Increasing sputter power and decreasing target-substrate distance leads to an increased deposition rate. To a lesser extent, lower substrate temperature and lower pressure also lead to a higher deposition rate.

Surface velocity determines the density and crystallinity of the film. When sputtered material, say, a few atoms, from a target reaches the substrate, there are three possibilities for the location at which that material will finally reside. This is illustrated in Figure 8. The material at location 1 hits the substrate and comes to rest somewhere away from the rest of the previously deposited material. This may then act as a nucleation point to which other depositing material may attach itself. At location 2, the depositing atoms come to rest on top of previously deposited layers. Material at location 2 will also serve as a nucleation point. Material at location 3 has deposited to the previously deposited material in such a way as to extend the lattice in an orderly fashion.

A higher surface velocity of depositing material allows the material to travel to a more favorable location before bonding to the rest of the film. The depositing material is then more likely to bond to dangling bonds on the surface of the film. This, in turn, leads to more ordered lattice structure. In general, surface velocity increases with increasing substrate temperature, increasing sputtering power, decreasing ambient pressure, and decreasing target-substrate distance. All of these factors increase the energy of depositing material at the substrate surface.

Figure 8: Material deposition on substrate.

If the energy of the depositing material is too high, however, the film could be damaged by the impact of the depositing material. Depositing material can imbed itself into the previously deposited film to form fractures and dislocations. Ion bombardment from the plasma can have the same effect. If controlled, however, ion bombardment can have a beneficial etching effect as well as contribute to surface velocity of depositing material. Higher sputtering power, lower pressure, and shorter target-substrate distance all lead to higher ion and sputtered material bombardment. Clearly, one of the goals of good sputter

deposition is to balance the effects of high surface velocity, which leads to high density films with large grains, and high material and ion impact, which leads to material damage.

4.1.3 TRIODE SPUTTERING

In the above described diode sputtering, there is a certain amount of ion and electron bombardment of the substrate which comes from the plasma. The amount of bombardment depends on ambient pressure, sputtering power, and substrate-target distance. In some applications, a negative DC bias may be applied to the substrate to increase ion bombardment. Other applications vary the magnetic field configuration to affect plasma confinement.[15]

Another way of controlling the bombardment of ions and electrons is to insert a grounded wire mesh between the target and substrate as in Figure 9. The mesh acts to block ions and electrons from the substrate while allowing the neutral sputtered material to pass through to the substrate. The substrate is grounded or negatively DC biased in order to control ion bombardment.

4.2 $CdCl_2$ Vapor Annealing System

In room 253 of ASC I at ISU, a system for annealing CdTe films in the presence of $CdCl_2$ and oxygen was built, modeled after McCandless.[11] The purpose of this system was explained in the first section. A diagram of the annealing system is shown in Figure 10. Inside a furnace tube is an ampoule where $CdCl_2$ powder and the CdTe sample are placed according to the diagram. The ampoule is kept outside of the furnace while it heats to the appropriate temperature (425°C in this study). The furnace tube is evacuated. Then, Ar and O_2 are introduced into the system (30% O_2 in this study). The ampoule is put into the furnace, where the $CdCl_2$ sublimes, and the vapor passes over the sample. The CdTe reacts with the vapor and anneals to produce an oxygen-doped film with large grains. One end of the ampoule is closed off, and the other end is packed with quartz wool. The wool serves as a surface on which CdO and other potentially hazardous end products of the reaction can deposit without entering the rest of the system. The anneal time was 30 min in this study.

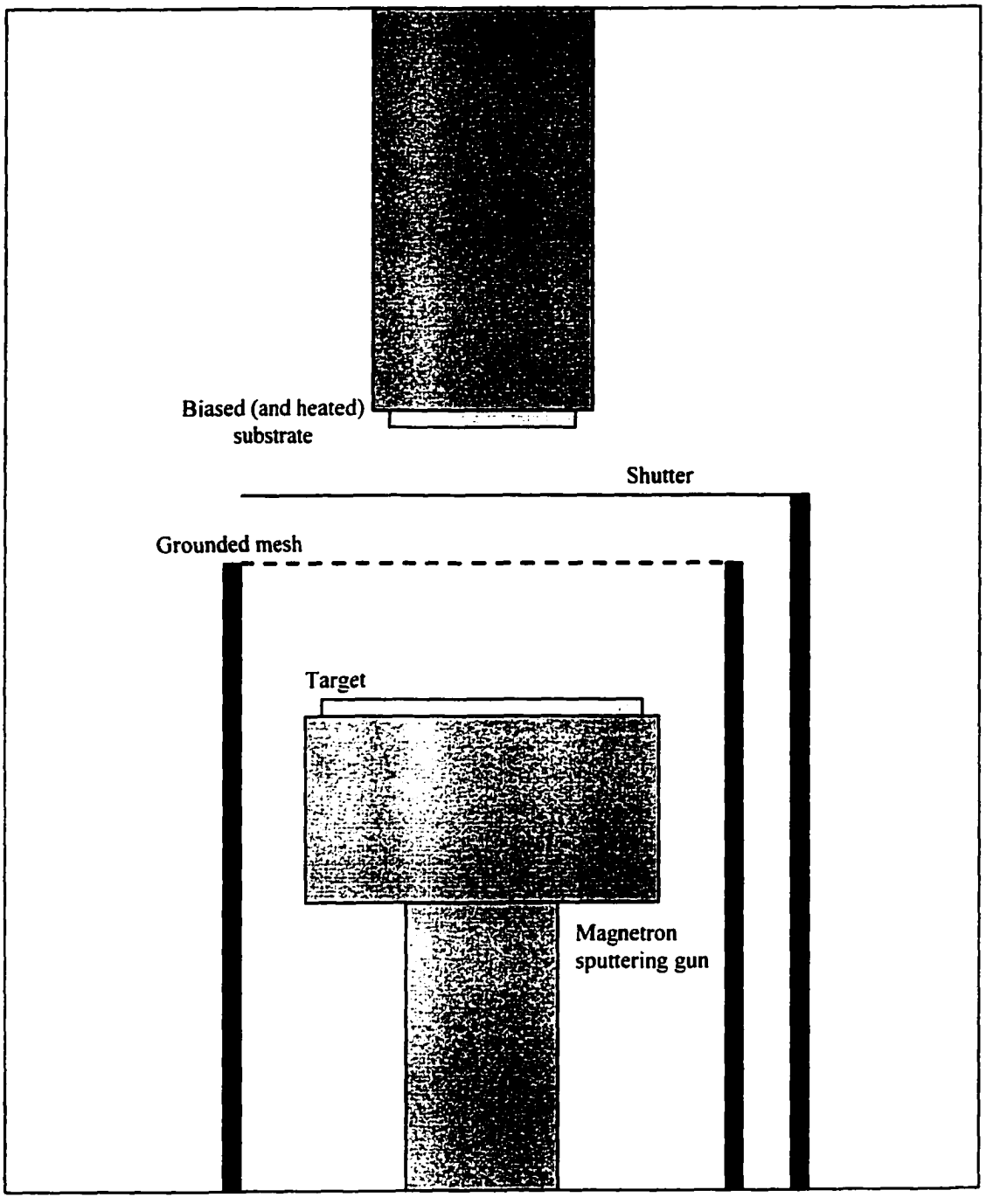

Figure 9: Triode sputtering system.

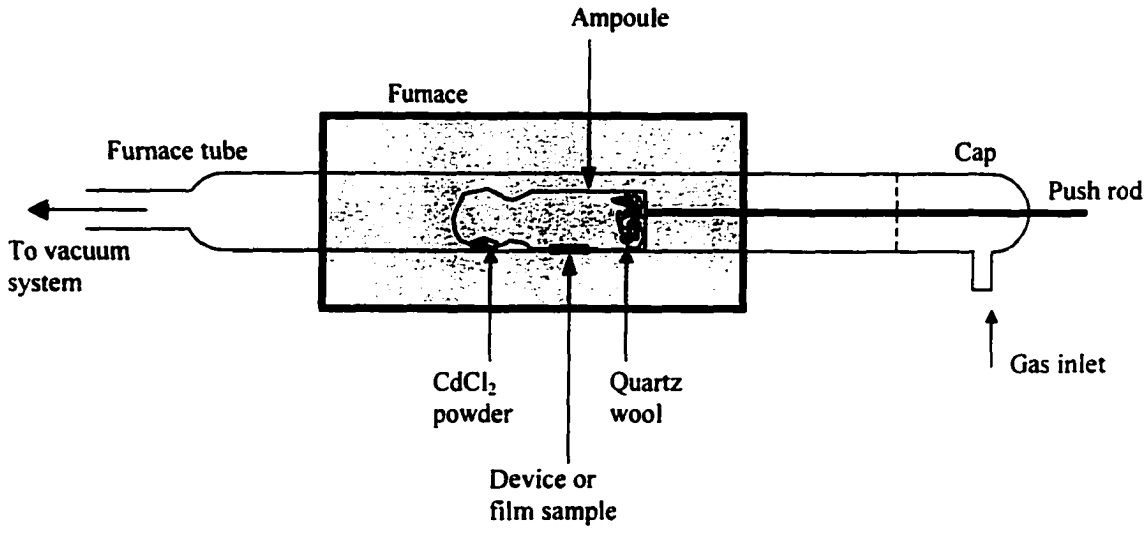

Figure 10: $CdCl_2$ vapor anneal system.

CHAPTER 5: CHARACTERIZATION TECHNIQUES

5.1 Material Characterization

5.1.1 THICKNESS

Reflectance was measured using a Perkin-Elmer Lambda-9 dual beam spectrophotometer. A beam of monochromatic light is generated and split into two separate beams. One beam is used as a reference for comparison with the second beam, which interacts with the sample film. A thin film with an incident beam and reflected beams is shown in Figure 11. The reflected beams will interfere constructively and destructively depending upon the thickness of the film and the wavelength of light. Assuming the film and substrate to be non-absorbing in the range of wavelengths measured, thickness is given by[16]

$$t = \frac{i\lambda_o\lambda_i}{2n(\lambda_i - \lambda_o)\cos(\phi)}$$

where n is the index of refraction, and i is the number of cycles from λ_o to λ_i, the two wavelength peaks that bracket the i cycles. For two adjacent peaks or two adjacent troughs, $i = 1$. In the application presented in this paper, the incident and reflected beams are normal to the plane of the film, making $\cos(\phi) = 1$. The range of wavelengths used was from 1000nm to 2500nm.

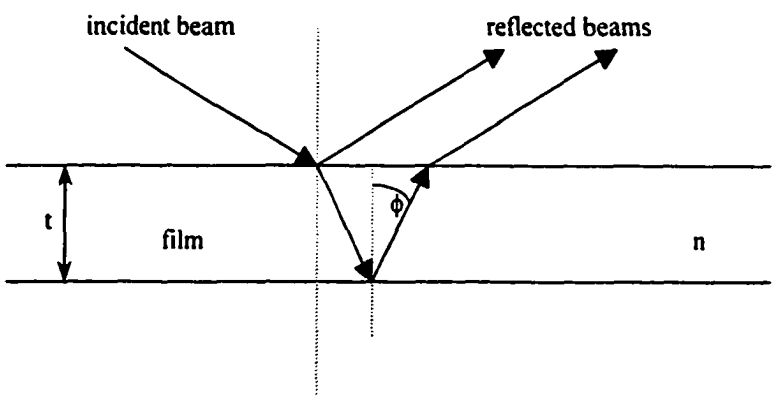

Figure 11: Reflected light on a thin film.

5.1.2 SCANNING ELECTRON MICROSCOPY (SEM)

The scanning electron microscope used for this work was a JEOL 6100 SEM. SEM is similar to light microscopy, except that electrons are used instead of photons. Since electron wavelengths are much smaller than photon wavelengths, much larger magnifications are possible. SEM produces a larger depth of field as well. An image is produced by scanning a beam of electrons over the surface of the sample and detecting the secondary or backscattered electrons. In this study, the SEM was used to examine the surface of CdTe films deposited at various parameters. Grain size and density, as well as surface roughness, are seen with SEM.

5.1.3 ENERGY-DISPERSIVE SPECTROSCOPY (EDS)

Energy-dispersive spectroscopy is a specific function of SEM. As the electron beam hits atoms in the sample, the electrons in the atoms are excited to higher energy levels. Those electrons then relax and emit photons. These photons are in the X-ray region of the spectrum. If the SEM is fitted with a proper detector (as the JEOL 6100 is), these X-rays can be collected and an EDS spectrum of the sample can be formed. Each element has characteristic wavelengths at which X-rays will be emitted. An EDS scan can therefore be used to help identify elements present in a sample. Relative concentrations of each element can also be determined by analyzing the intensities of the peaks. In this study, EDS was used to determine Cd/Te ratios in CdTe films, as well as O and Cl content.

5.1.4 X-RAY DIFFRACTION (XRD)

A Siemens X-ray diffractometer was used in this study. The principles of XRD are based on Bragg's diffraction law, given by

$$2d \sin\theta = n\lambda,$$

where n is an integer. A monochromatic X-ray of wavelength λ is incident on a sample. In this study, Cu Kα X-rays with $\lambda = 1.542$Å were used. The sample contains lattice planes separated by a distance d at an angle θ. Constructive interference occurs only when the distance traveled by the X-rays reflected from successive planes differs by exactly n wavelengths. The thin films studied here are polycrystalline, with grains of various orientations. By varying θ, the Bragg condition is satisfied by different d-spacings,

depending on the orientations of the grains. Plotting the angular positions and intensities gives a pattern characteristic of the sample. The plot will show peaks at various angles (usually, intensity vs. 2θ is plotted) corresponding to specific orientations of the given material. Therefore, XRD can be used to show relative concentrations of the various orientations of the sample. In this study, XRD was performed on CdTe films to show just that.

5.1.5 PHOTOLUMINESCENCE (PL)

In a photoluminescence (PL) measurement the sample is placed in a cryostat and cooled to temperatures as low as that of liquid He. The sample is excited with an optical source with $h\nu > E_g$. In this study, the samples are CdTe films, and the optical source is a He-Ne 632.5nm laser. This generates electron-hole pairs that recombine by one of several mechanisms. In general, the recombination process is either radiative (emitting a photon), or non-radiative (no photon is emitted). Low-temperature measurements are necessary to minimize thermally-activated non-radiative recombination processes. Photons from the radiative recombination events are collected by a detector. In this study, an Ocean Optics photodetector was used. Generally, a lack of PL signal can indicate the presence of deep defect levels in the bandgap.

5.1.6 RAMAN SPECTROSCOPY

Raman spectroscopy measurements were performed on ZnTe films according to reference 17 by Akhlesh Gupta at the University of Toledo. In Raman measurements, laser light incident on the measured material interacts with optical phonons from the crystal lattice of that material. If an incident photon gives part of its energy to the lattice in the form of a phonon, it emerges as a lower-energy photon. This is known as Stokes-shifted scattering. This light is detected by a photodetector after passing through a double monochromator. Each material has a characteristic Raman spectrum associated with it. The sharpness and intensity of the various peaks indicate the composition and crystallinity of the material.

5.1.7 FOUR-POINT PROBE

The arrangement for a four-point probe measurement consists of four collinear probes. A current is passed between the outside two probes, and the voltage drop is measured across the inside probes. It can be shown that for a sample where the thickness is less than or equal to half the probe spacing, the sheet resistance is given by[18]

$$R_s = \frac{\pi}{\ln(2)}\frac{V}{I} = 4.532\frac{V}{I},$$

where V and I are the voltage and current, respectively. Resistivity and conductivity can then be found by

$$\rho = R_s t, \text{ and } \sigma = \frac{1}{\rho},$$

where t is the film thickness found from reflection measurements. The four-point probe measurement is not suitable for highly resistive samples. In this study, four-point probe measurements were performed on highly doped p^+-ZnTe films and n^+-CdS films.

5.1.8 VAN DER PAUW MEASUREMENTS

An alternative, but closely related method for resistivity measurement is the Van der Pauw method. The resistivity of a flat sample of arbitrary shape such as that shown in Figure 12 can be determined if the following conditions are met: The contacts are at the circumference of the sample, the contacts are very small, the sample is of uniform thickness, and the sample is singly connected (there are no isolated holes).

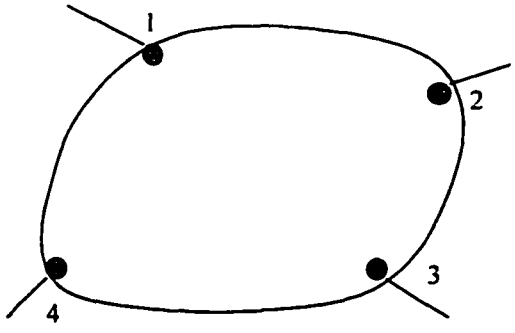

Figure 12: Sample material to be measured with van der Paw measurement.

Resistivity is measured in the following manner. Current is passed through two adjacent contacts while voltage is measured across the remaining two contacts. Let $V_{AB,CD}$ denote V_D-V_C when current enters at contact A and leave at B. Then the following voltages are measured and averaged (V_{avg}) as the magnitude of the current, I, is kept constant: $V_{12,34}$, $V_{23,41}$, $V_{34,12}$, and $V_{41,23}$. Then the average resistance is

$$R_{avg} = \frac{V_{avg}}{I}.$$

Sheet resistance can be found by

$$R_s = 4.53 \cdot CF \cdot R_{avg}$$

where CF is a correction factor nearly equal to 1. Resistivity is then found by

$$\rho = R_s \cdot t$$

where t is the sample thickness.

5.1.9 ACTIVATION ENERGY

Dark conductivity measured as a function of temperature gives an indication of the crystallinity and doping density of a material. The activation energy of a polycrystalline material is the energy required for carriers to surmount energy barriers at grain boundaries, and is found by

$$I = I_0 \exp\left(-\frac{E_a}{kT}\right).$$

Taking the negative of the slope of a plot of $\ln(I)$ vs. $1/kT$ gives the activation energy. In this study, unless otherwise stated, activation energy is measured on p^+-ZnTe films with a bias of 1V and at temperatures starting at 205°C and going down to 130°C.

5.2 Device Characterization

5.2.1 CURRENT-VOLTAGE (I-V) CHARACTERISTICS

The current-voltage relationship can be expressed by the following equation, assuming no series resistance and an infinite shunt resistance:

$$I = I_o\left[\exp\left(\frac{-qV}{kT}\right) - 1\right] - I_L.$$

The reverse saturation current, I_o, of the diode is given by

$$I_o \approx \frac{qn_i w_D}{2\tau},$$

where n_i is the intrinsic carrier concentration, w_D is the depletion width, and τ is the minority carrier lifetime. In the case of CdS/CdTe solar cells, the minority carriers in CdTe are electrons. Here it is seen that a shorter depletion width and longer lifetime both lead to smaller saturation current. The light current, I_L, is given by

$$I_L = (1-R)\int q \cdot QE(\lambda) \cdot \frac{dN_{ph}(\lambda)}{d\lambda} d\lambda,$$

where R is the fraction of reflected light, λ is wavelength, QE is the quantum efficiency of the device at a given wavelength, and N_{ph} is the number of photons in the spectrum at a given wavelength. Therefore, it is seen that higher quantum efficiency gives increased light current.

The equivalent circuit of a non-ideal solar cell is shown in Figure 13. The circuit consists of a current source, a diode, series resistance, and shunt resistance. The current source represents the current generated from illumination. Series resistance comes from bulk resistance of the materials in the diode as well as resistance of the contacts and interconnects. Shunt resistance can be caused by lattice defects in the depletion region such as grain boundaries and large precipitates. Also, shunt resistance can come from leakage currents around the edge of the cell. If shunt resistance is finite and series resistance is non-zero, the current voltage relationship becomes

$$I = I_o\left\{\exp\left[\frac{q(V-IR_s)}{kT}\right]-1\right\}+\frac{V-IR_s}{R_{sh}}-I_L,$$

where A is the area of the cell, R_s is series resistance, and R_{sh} is shunt resistance. The performance of a solar cell can be completely described by the current-voltage relationship. A typical current voltage curve is shown in Figure 14. Although the values of current are shown to be positive in the 'up' direction of the graph, it is understood that the current is negative in the 'up' direction. The slope of the curve near point A is nearly $1/R_s$, while the slope near point B is $1/R_{sh}$.

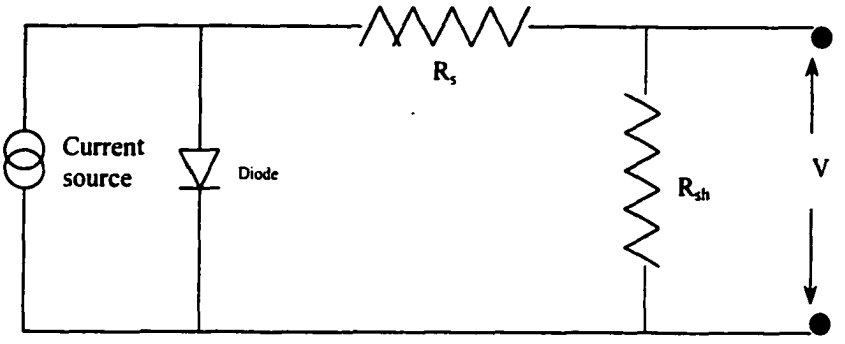

Figure 13: Equivalent circuit of solar cell.

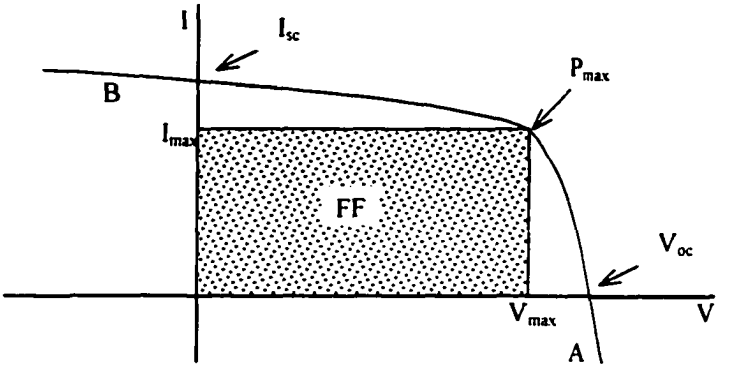

Figure 14: I-V curve of typical solar cell.

For practical purposes, it is sufficient to characterize the current voltage dependence with only three parameters. The first one is the short-circuit current, I_{sc}, which is obtained from the previous equation for $V = 0$. For a solar cell with $R_s = 0$, it is clear that $I_{sc} = I_L$. A non-zero R_s reduces I_{sc}.

A second parameter is the open-circuit voltage, V_{oc}, which is obtained for $I = 0$. Solving for V with $I = 0$ leads to a transcendental equation which can only be solved numerically. However, in the ideal case of infinite R_{sh} and $R_s = 0$, V_{oc} can be expressed as

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_L}{I_s} + 1\right).$$

Thus, increased I_L and decreased I_s leads to increased V_{oc}. Furthermore, a finite R_{sh} will lower V_{oc}.

The third parameter typically used to characterize solar cells is the fill factor, FF. The performance of the solar cell is eventually determined by the fraction of the total power of incident light that can be converted into electrical power. The solar cell will be operated under conditions that give maximum power output. The maximum possible area $P_{max} = V_{mp}I_{mp}$ as shown in Figure 14 determines FF given by

$$FF = \frac{V_{mp} I_{mp}}{V_{oc} I_{oc}}.$$

This is a measure of the "squareness" of the I-V curve.

5.2.2 QUANTUM EFFICIENCY

Quantum efficiency (QE) is defined as the ratio of the number of carriers collected as current (per unit time) to the number of photons incident on the solar cell (per unit time). The QE of a solar cell is a function of the wavelength of the incident photons. The measurement apparatus used is illustrated in Figure 15. A light source is shone through a monochromator, which produces a light beam with nearly a single wavelength. This wavelength can be varied. In this study, the wavelengths used ranged from 400 to 940 nm. The resulting light beam is directed through a chopper to produce a square wave with a frequency of ~13.5 Hz. This reduces noise due to ambient light and 60 Hz power lines. A high-pass filter is set in the beam's path for wavelengths greater than 700 nm to eliminate photons of shorter wavelength. The beam is focused with lenses and directed by a mirror onto the sample under test. Probes are contacted to the front and back contacts to apply a bias, if desired, and to read the current resulting from the incident light beam. The current is converted to a scaled voltage signal which is sent to a lock-in amplifier tuned to the chopper frequency. With knowledge of the scaling factor, the voltage signal readout can then be converted back to current.

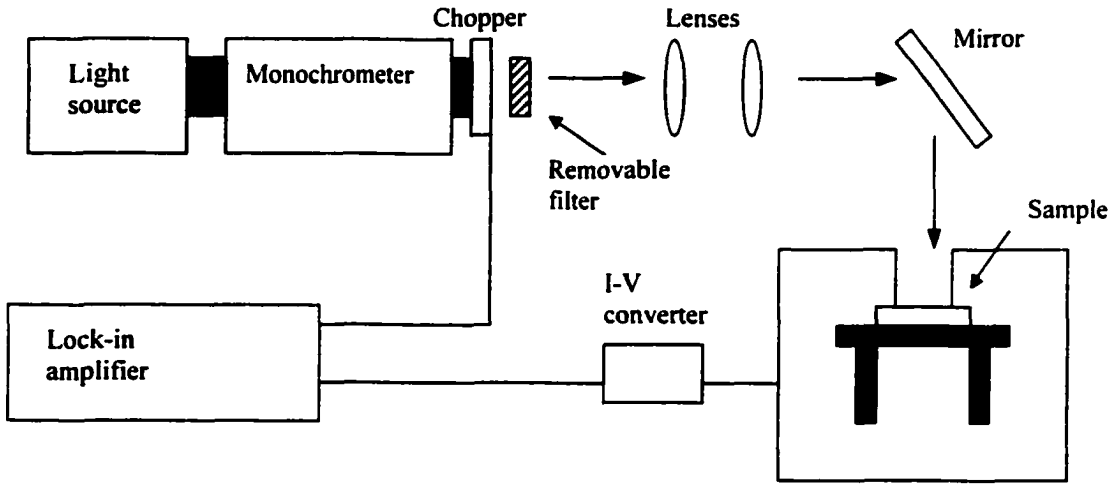

Figure 15: Quantum efficiency measurement apparatus.

Both the sample, and a reference photodiode with a known QE, η_{ref}, at the measured wavelengths, are measured in the manner described above. The QE, η_{sam}, of the sample under test can be found by

$$\eta_{sam} = C\frac{I_{sam}}{I_{ref}}\eta_{ref},$$

where I_{sam} and I_{ref} are the current readings for the sample and reference, respectively. The constant, C, depends on the ratio of the areas of the sample and reference, as well as on the lens positioning and location of the reference compared to the sample. In this study, the reference and sample are in different locations with different lens and mirror positions. This means that the number of photons incident on the reference is not the same at that of the sample. Therefore, QE for the sample is computed from the above equation without the constant, and the value is a relative value to be compared from wavelength to wavelength of a given device, as well as from sample to sample. In a typical QE spectrum, the maximum value is set to 1 with the rest scaled accordingly.

Measuring QE under bias gives information about the electric field profile and material and junction quality of a solar cell. Under forward bias the internal electric field is reduced. Consequently, the carrier collection efficiency (and therefore the QE) is reduced

due to the dependence of carriers on the electric field to be collected as current. Likewise, under reverse bias the electric field will increase and cause an increase in the collection efficiency. An increase in the QE with reverse bias and a decrease with forward bias will show that photons are absorbed, but the carriers generated are not able to reach the junction without an assist from the electric field. This gives an indication of the material and junction quality.

Comparing the differences in QE(bias)/QE(ground) ratios at various wavelengths gives information about the absorption characteristics with respect to distance from the junction. If, for example, under forward bias, the QE ratios at long wavelengths are smaller than those at short and middle wavelengths, then photons are generating carriers far from the junction, but the carriers are not being collected without an electric field assist. If the QE ratios are smaller at the short wavelengths, a problem exists at the junction. Comparison of the QE ratio levels of different devices will also give a comparison of the electric field quality of one device to another.

In this study, unless otherwise stated, the phrase "QE ratio" refers to the ratio QE(0.4V)/QE(0V).

CHAPTER 6: RESULTS AND DISCUSSION

6.1 Triode Sputtering of CdTe Films.

CdTe films were deposited on 0.1mm thick Mo substrates using triode sputtering. The target and substrate were spaced 6 cm apart, with the wire mesh directly in between them. Substrate temperature, ambient pressure, and substrate bias were varied. It should be noted that throughout this paper, when bias is mentioned, it refers to substrate bias during deposition. Post-deposition treatment was then performed with the $CdCl_2$ vapor anneal described in chapter 4. Structural analysis was performed using SEM, XRD, and PL measurements. Superstrate devices were fabricated with limited, but still somewhat enlightening, results.

6.1.1 SEM ANALYSIS.

Figures 16–19 show 5000x SEM images of CdTe films deposited with 2mTorr pressure pure Ar and 380°C substrate temperature. The film in Figure 16 was grounded, while Figures 17, 18, and 19 were biased at –2V, –12V, and –36V, respectively.

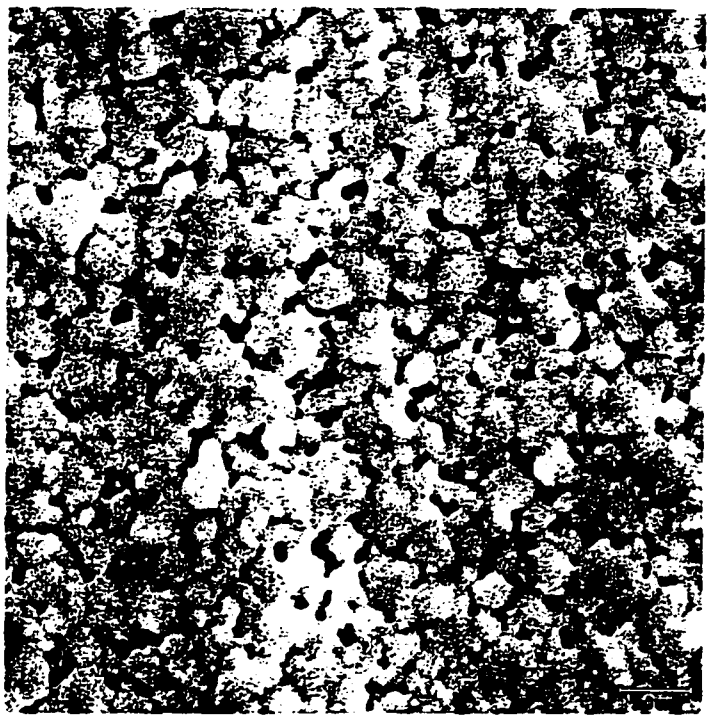

Figure 16: SEM of CdTe film deposited with no bias at 2mTorr.

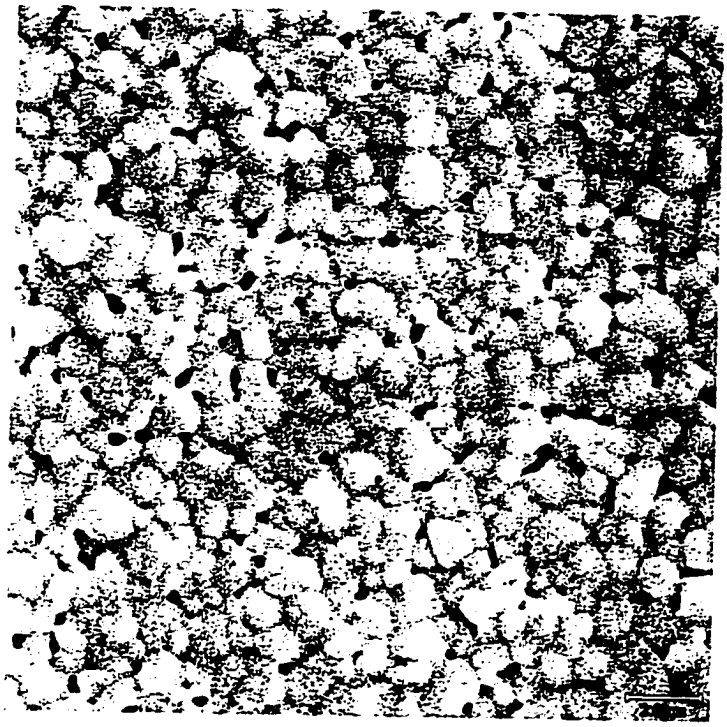

Figure 17: SEM of CdTe film deposited with –2V bias at 2mTorr.

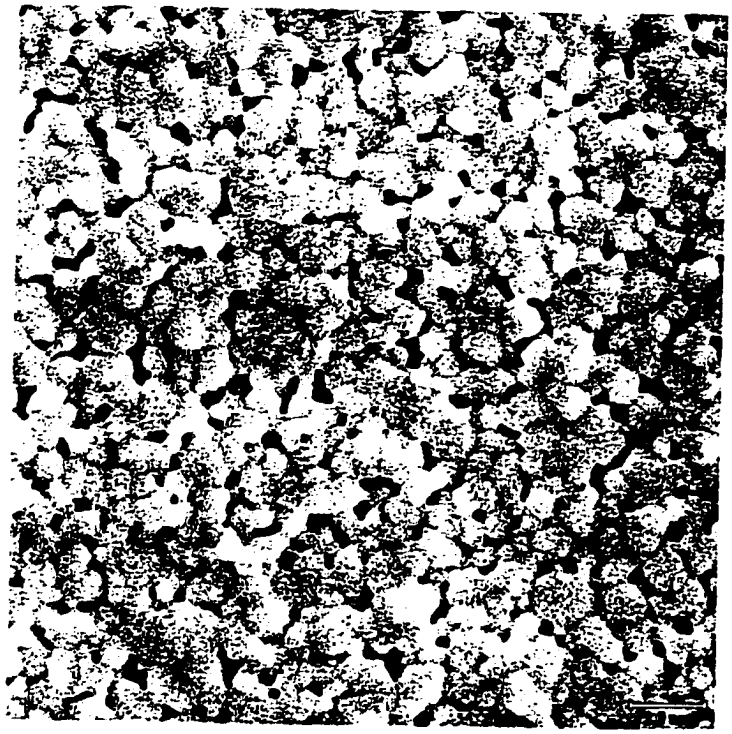

Figure 18: SEM of CdTe film deposited with –12V bias at 2mTorr.

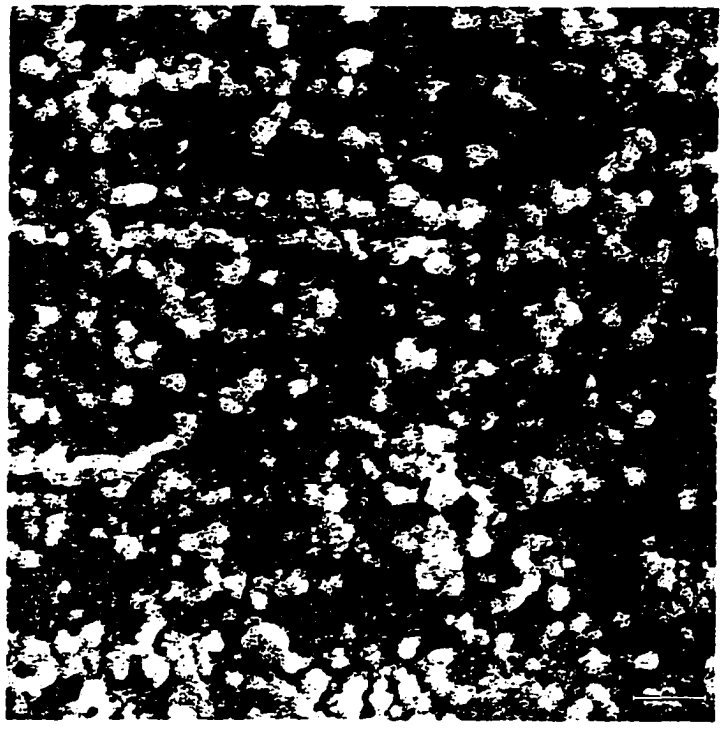

Figure 19: SEM of CdTe film deposited with –36V bias at 2mTorr.

Immediately evident is the fact that the film deposited at –36V bias is nearly non-existent. The bias appears to have a severe etching effect from increased ion bombardment at the substrate during deposition. Thickness measurements confirm the lack of film on the substrate. There is some amount of film left at the edge, which is about 0.5in from the center. However, what is left is severely blistered.

The remaining films appear to be fairly similar. The film deposited with a –2V bias seems to have more closely packed grains than the other films. A –12V bias yielded films with the largest number of gaps between grains. This is a repeatable result and may be due to the following. A "small" amount of ion bombardment from a "small" substrate bias would be enough to increase the surface mobility of the material being deposited so as to produce a more tightly packed film than one deposited with no bias. A "large" amount of ion bombardment from a "large" substrate bias would have the effect of etching the film during deposition, creating a rough surface. This effect is seen with the film deposited with –36V

bias. Thickness measurements confirm that an increase in bias magnitude leads to etching during deposition. See Figure 20.

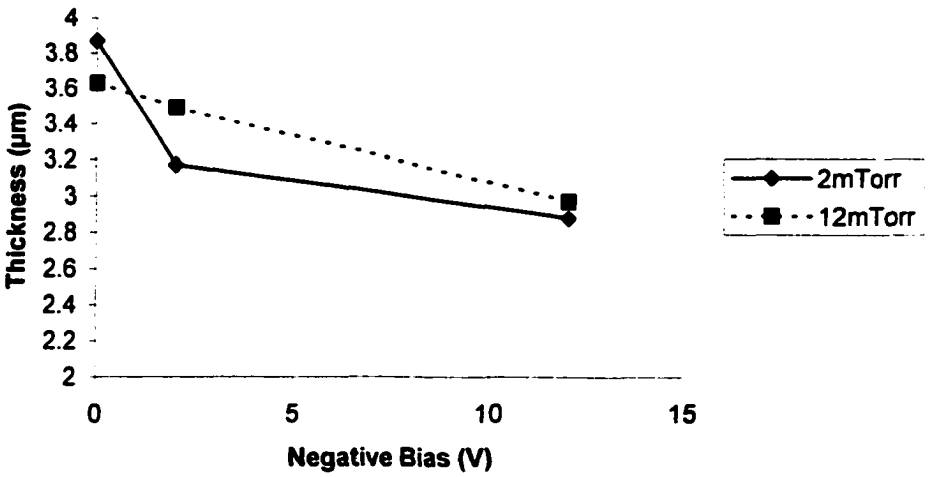

Figure 20: Thickness vs. substrate bias for 2mTorr and 12mTorr films.

The image of the film deposited with 0V bias (Figure 16) shows small white "bumps" on the grains. These bumps appeared on many films with no apparent correlation to deposition conditions. Focusing in on one of these bumps to perform an EDS scan revealed an abundance of oxygen. This indicates an oxide on the surface, likely formed during the $CdCl_2$ heat treatment. Cadmium oxide is typically formed on the surface of the film during the heat treatment, and is easily removed from the surface with a dip in a Br:methanol solution. The white bumps, however, did not disappear with a Br:methanol dip. Tellurium oxide, therefore, is the most likely material contained in these bumps. No effort was made to eliminate these bumps, as optimization of the heat treatment process was not the focus of this study.

Figures 21–23 show 5000x SEM images of CdTe films deposited with 12mTorr pressure pure Ar and 380°C substrate temperature. The film in Figure 21 was grounded, while those in Figures 22 and 23 were biased at –2V and –12V, respectively.

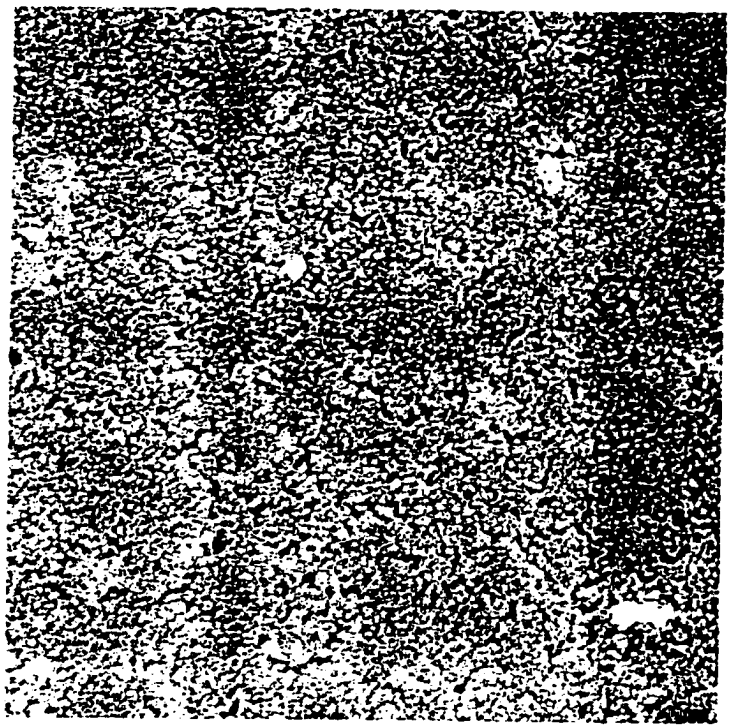

Figure 21: SEM of CdTe film deposited with 0V bias at 12mTorr.

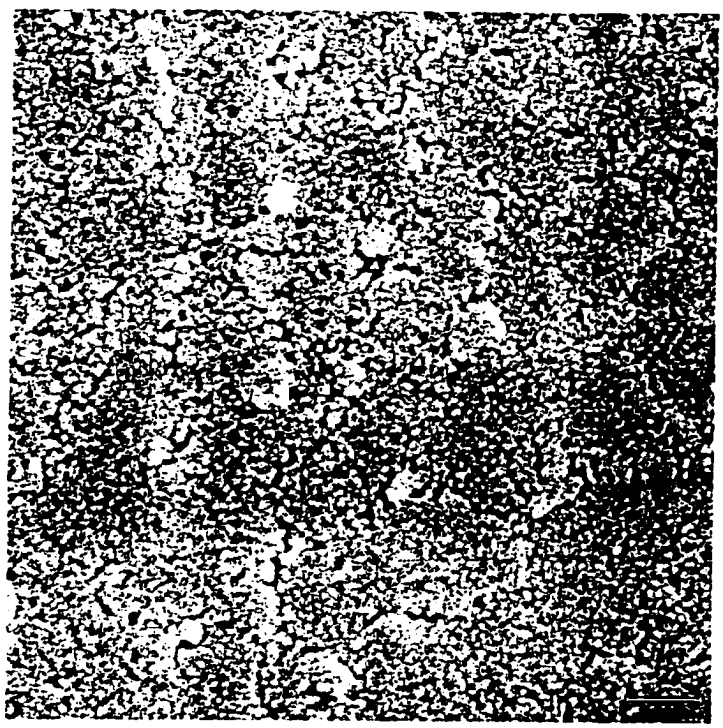

Figure 22: SEM of CdTe film deposited with –2V bias at 12mTorr.

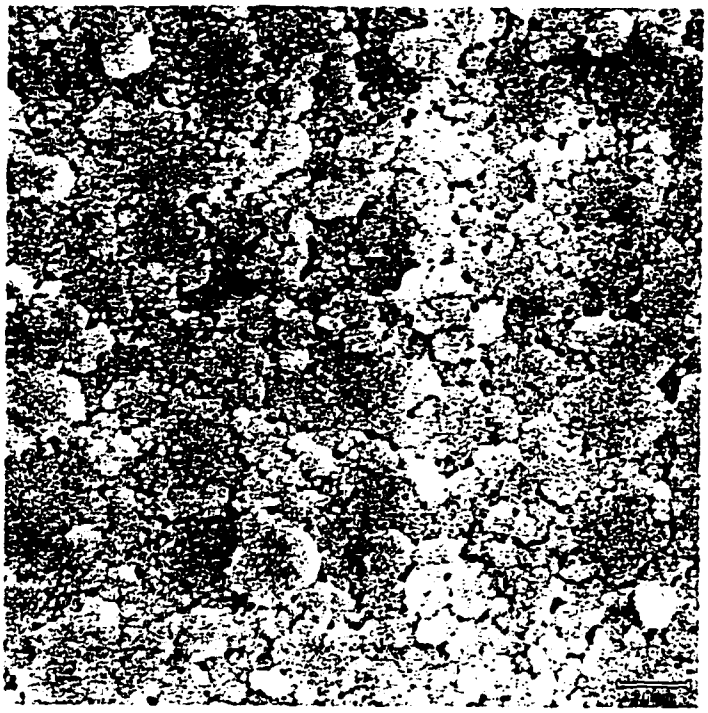

Figure 23: SEM of CdTe film deposited with –12V bias at 12mTorr.

The most striking observation is a comparison with the films deposited at 2mTorr. The 12mTorr films appear to have much smoother surfaces with poorly defined grain boundaries, which seems to indicate amorphous (or partly amorphous) films. Because of the higher deposition pressure, the material being deposited from the target onto the substrate has a shorter mean free path. This leads to a lower surface velocity (compared to that for the 2mTorr pressure) by the time the material reaches the substrate, and hence poorly defined grain boundaries.

At this higher pressure, a comparison of the changing bias shows that increasing the bias (magnitude) causes grain boundaries to become more well-defined. The most likely scenario is that increased ion bombardment of the substrate is increasing the surface velocity of depositing material. It should be noted that, as with the 2mTorr films, the 12mTorr films showed a decrease in thickness with increased bias, again due to ion etching during deposition. See Figure 20.

Figures 24–26 show 1000x SEM images of CdTe films deposited with 2mTorr pure Ar and –2V substrate bias. The films were deposited at 200°C, 300°C, and 400°C, respectively. Most noteworthy is the blistering that occurs on the 200°C film and, to a small extent, on the 400°C film. The blistering likely occurs during the anneal process. This might initially indicate that a higher deposition temperature is needed for the film to adhere to the substrate, since this increases the energy of the depositing material to form bonds. However, films deposited with 12mTorr pressure at various temperatures exhibited no blistering. Since the higher pressure actually takes away from the energy of the depositing material, it would seem that the energy of depositing material is not the sole determining factor in film blistering. It may be that, because films deposited at the higher pressure are not as structured as those deposited at the lower pressure, the material in the high-pressure films is better able to move itself around during the anneal without causing damage.

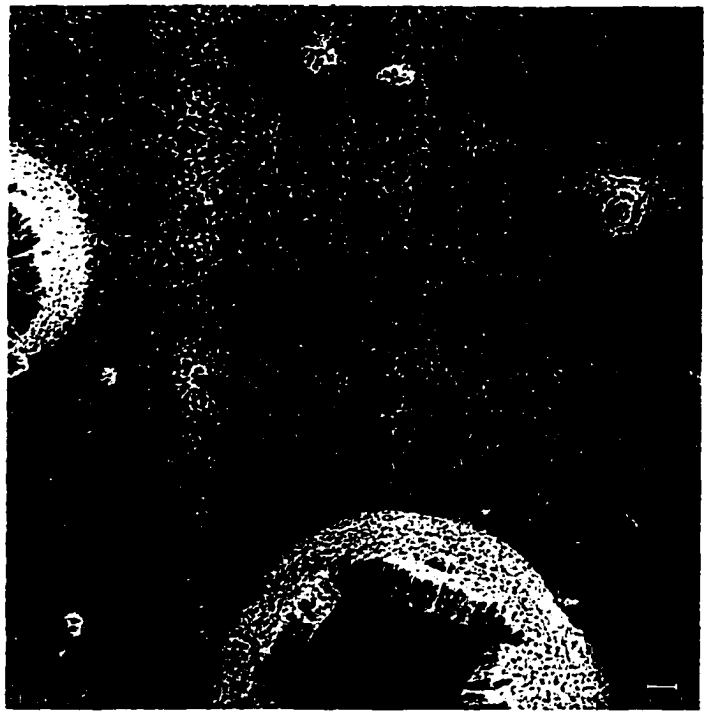

Figure 24: SEM of CdTe film deposited at 200°C.

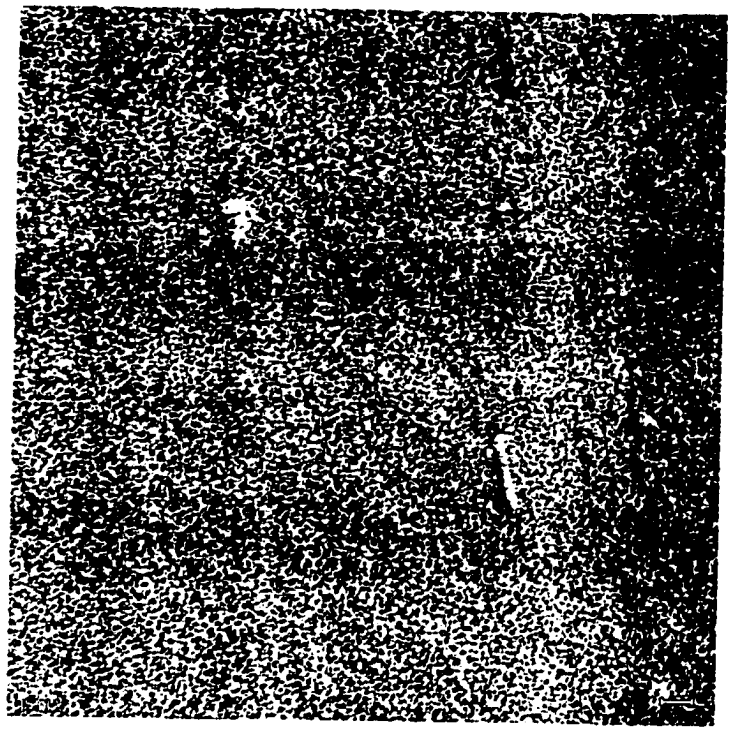

Figure 25: SEM of CdTe film deposited at 300°C.

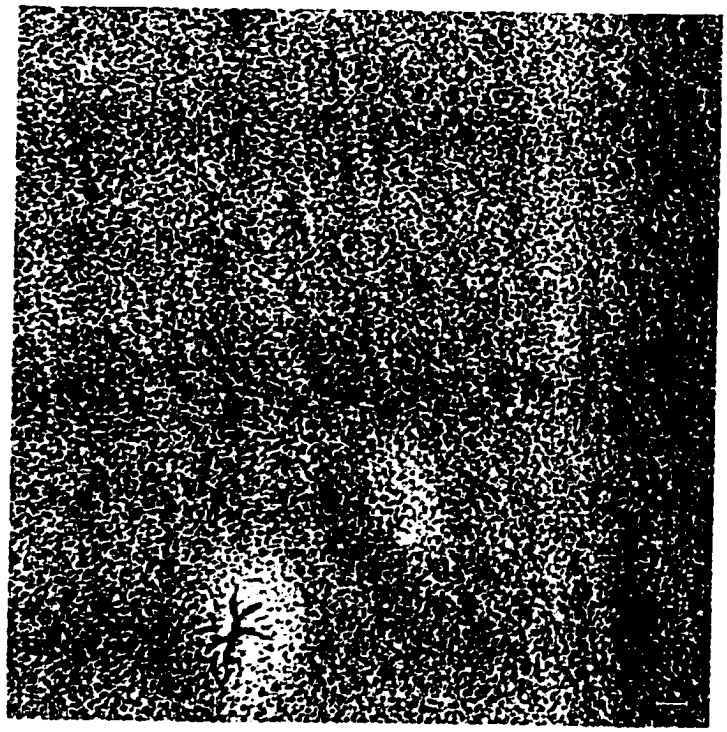

Figure 26: SEM of CdTe film deposited at 400°C.

6.1.2 XRD ANALYSIS.

Figures 27–29 show XRD spectra of films deposited at 2mTorr and 380°C, with biases of 0V, –2V, and –12V, respectively. The peaks at $2\theta = 23.75°$, 39.27°, and 46.41° correspond to CdTe grain orientations in the <111>, <220>, and <311> directions, respectively. The peak at $2\theta = 58.57°$ corresponds to a Mo peak, which is the substrate material.

Comparing relative peak intensity within each spectrum, all three films show the <311> peak as the largest in magnitude. There is no significant change in spectra from 0V to –2V substrate bias—only a slight decrease in the <111> peak, likely within experimental error. However, at –12V there is a significant increase in the <111> peak relative to the others, almost equaling the <311> peak magnitude. This suggests that substrate bias does affect grain structure, which was also evident from the SEM images.

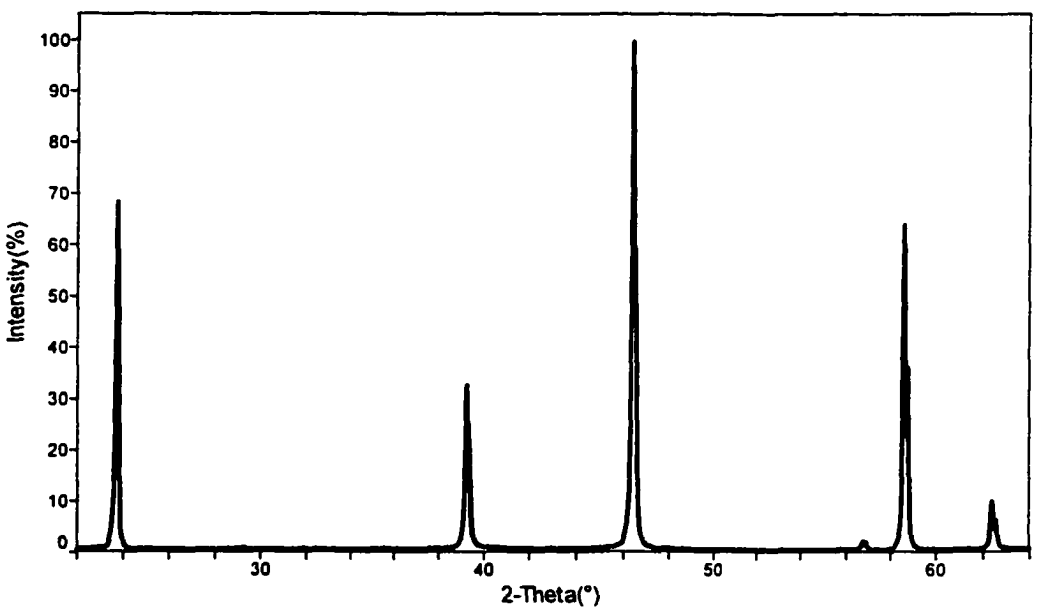

Figure 27: XRD of CdTe film deposited with no bias at 2mTorr.

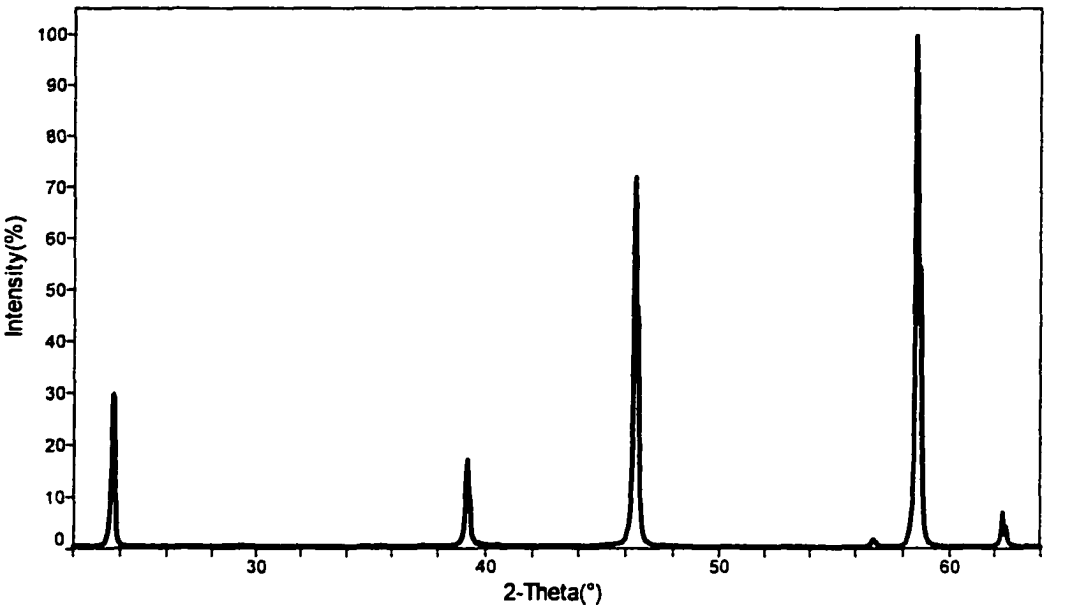

Figure 28: XRD of CdTe film deposited with –2V bias at 2mTorr.

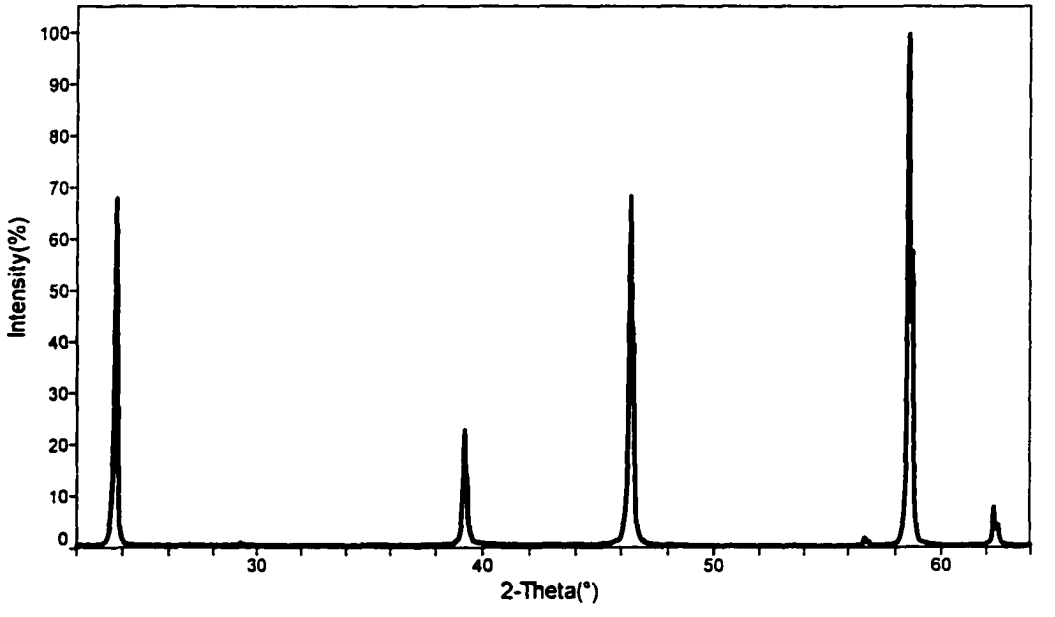

Figure 29: XRD of CdTe film deposited with –12V bias at 2mTorr.

Similar effects can be seen from analysis of films deposited in the same manner. but with 12mTorr pressure, as shown in Figures 30–32. These films also show a relative increase in the <220> peak with bias (where the 2mTorr films did not). At this higher pressure, the films become oriented much more randomly with bias. This seems to contradict the fact that the SEM images show an increase in grain definition with bias. One might think that an increase in grain definition indicates a more ordered structure, which should mean more uniformity in orientation. The XRD analysis indicates that this is not necessarily the case.

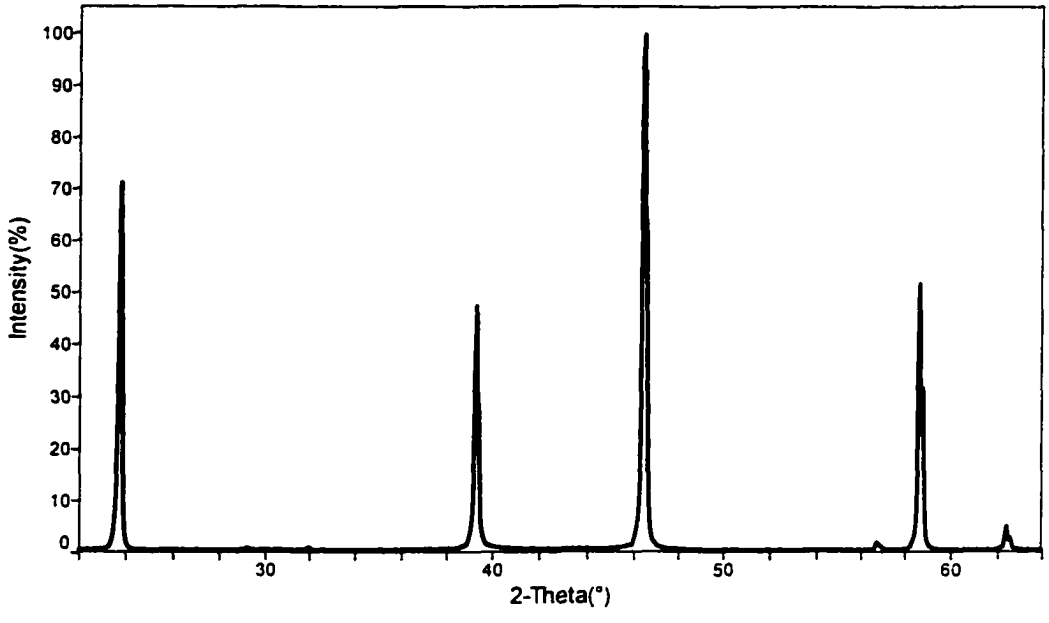

Figure 30: XRD of CdTe film deposited with no bias at 12mTorr.

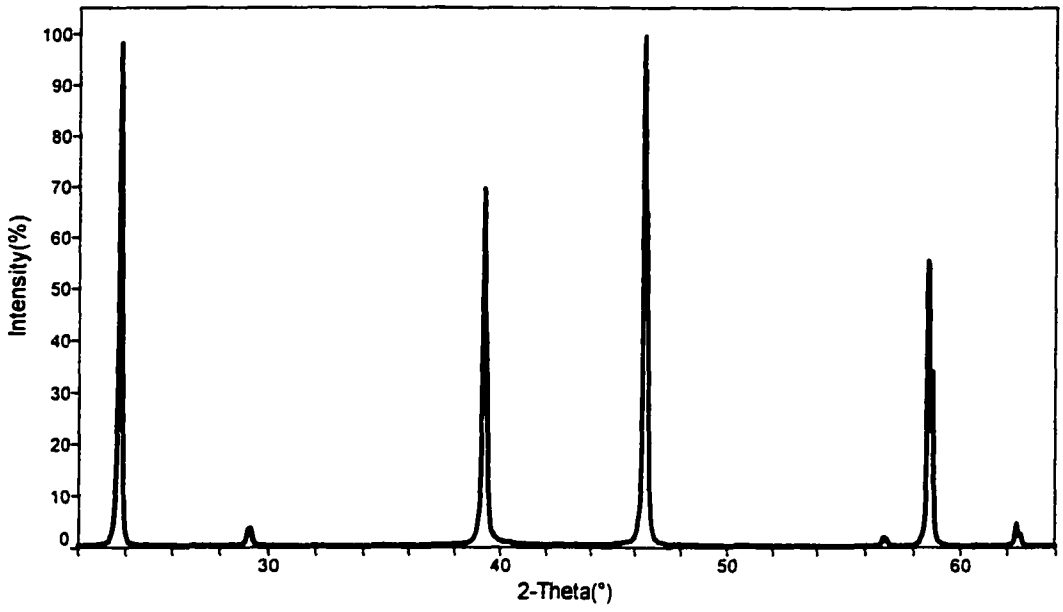

Figure 31: XRD of CdTe film deposited with –2V bias at 12mTorr.

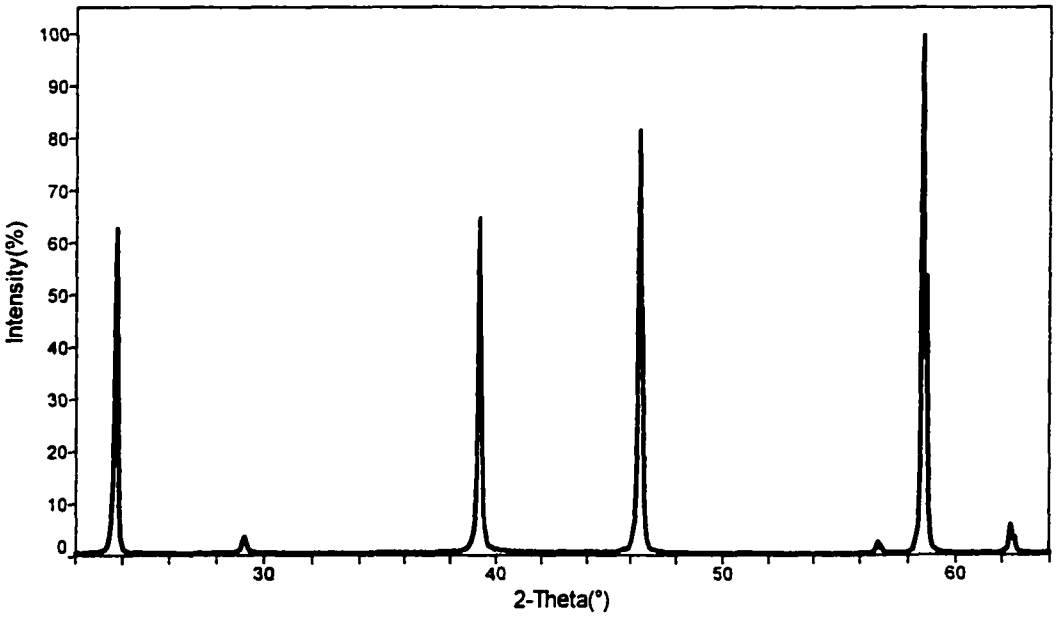

Figure 32: XRD of CdTe film deposited with –12V bias at 12mTorr.

Figures 33–35 show XRD spectra of CdTe films deposited with 2mTorr pressure and –2V substrate bias, at substrate temperatures of 200°C, 300°C, and 400°C, respectively. Here it is seen that the <311> peak increases (relative to the <111> peak) with temperature. Figures 36–38 show films deposited in the same manner, but with 12mTorr pressure. These figures show that at the higher pressure, it takes a higher deposition temperature to have any effects on the orientation. It is not until the 400°C deposition that increases in the other peaks relative to the <111> peak are observed. However, the trend is the same as with 2mTorr films. Again, an increase in random orientation is seen with an increase in the energy of the depositing material, whether this energy comes from ion bombardment or from substrate temperature. This is somewhat counter-intuitive, as an increase of energy to a system is usually associated with an increase in order.

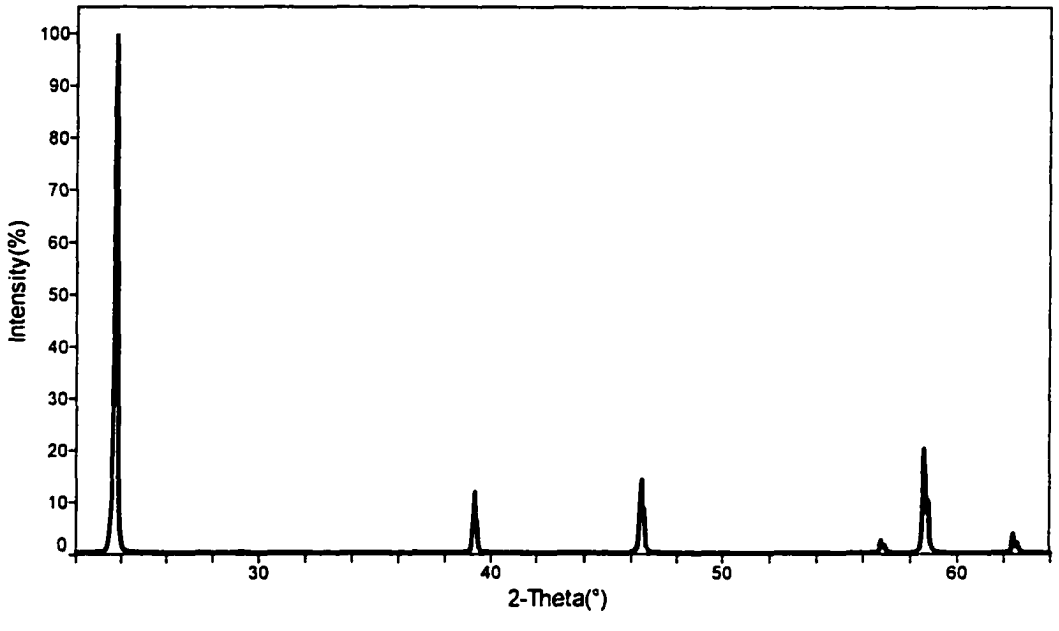

Figure 33: XRD of CdTe film deposited at 200°C at 2mTorr.

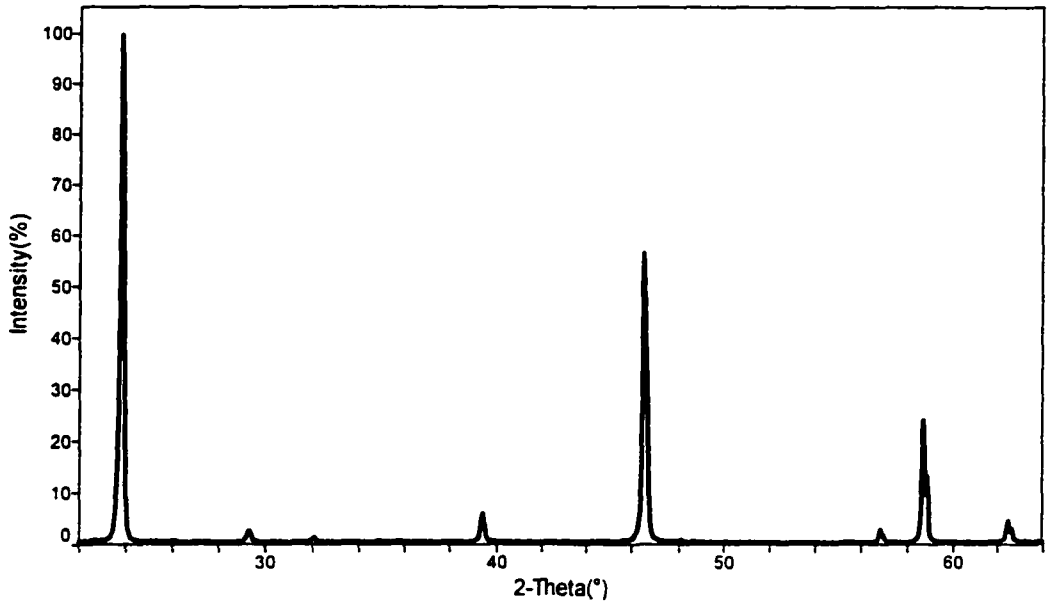

Figure 34: XRD of CdTe film deposited at 300°C at 2mTorr.

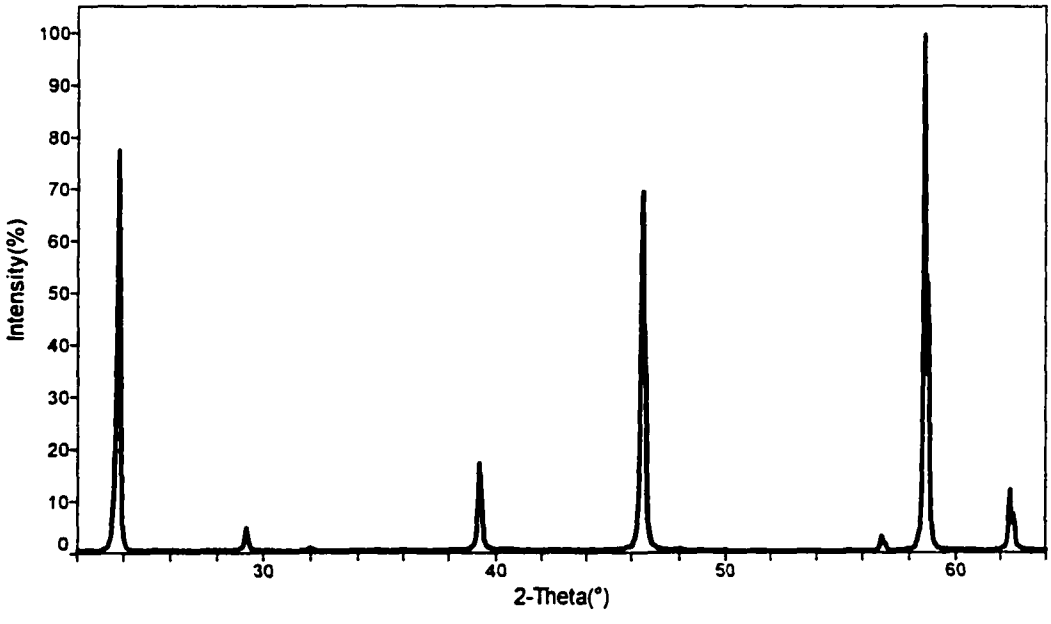

Figure 35: XRD of CdTe film deposited at 400°C at 2mTorr.

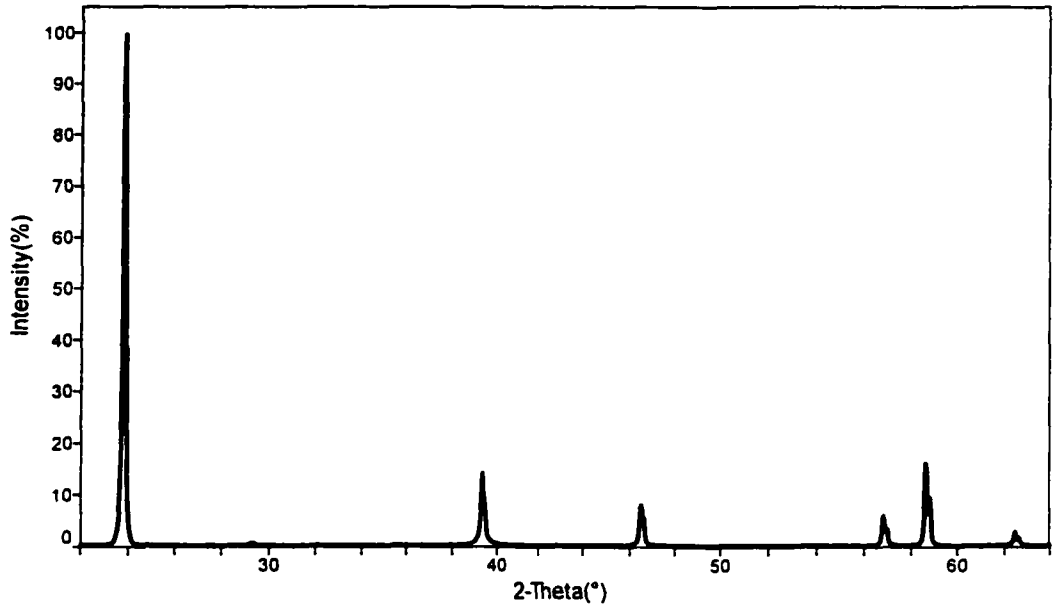

Figure 36: XRD of CdTe film deposited at 200°C at 12mTorr.

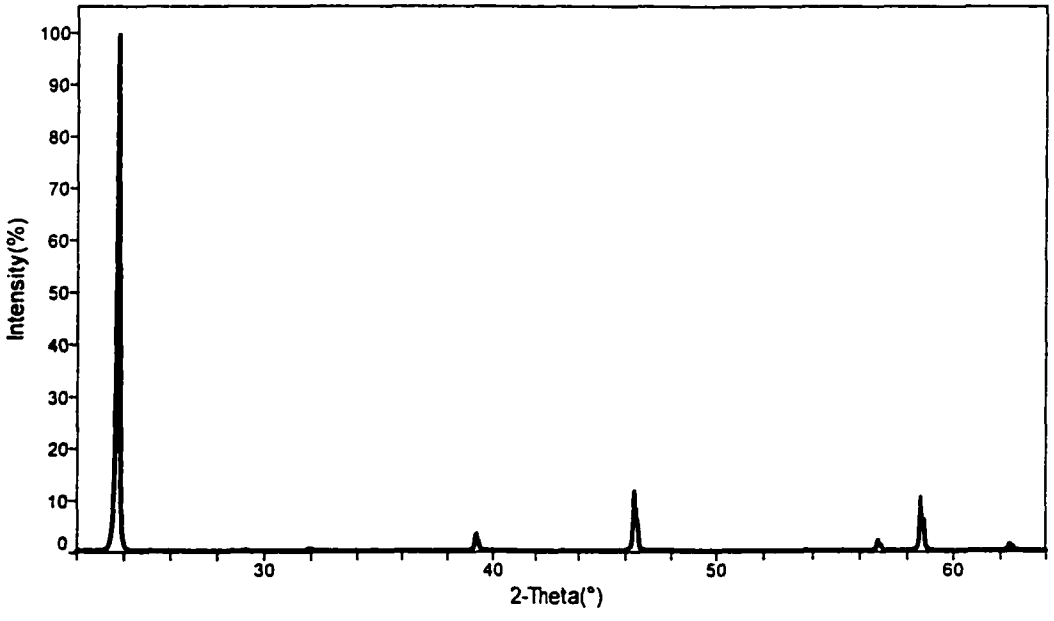

Figure 37: XRD of CdTe film deposited at 300°C at 12mTorr.

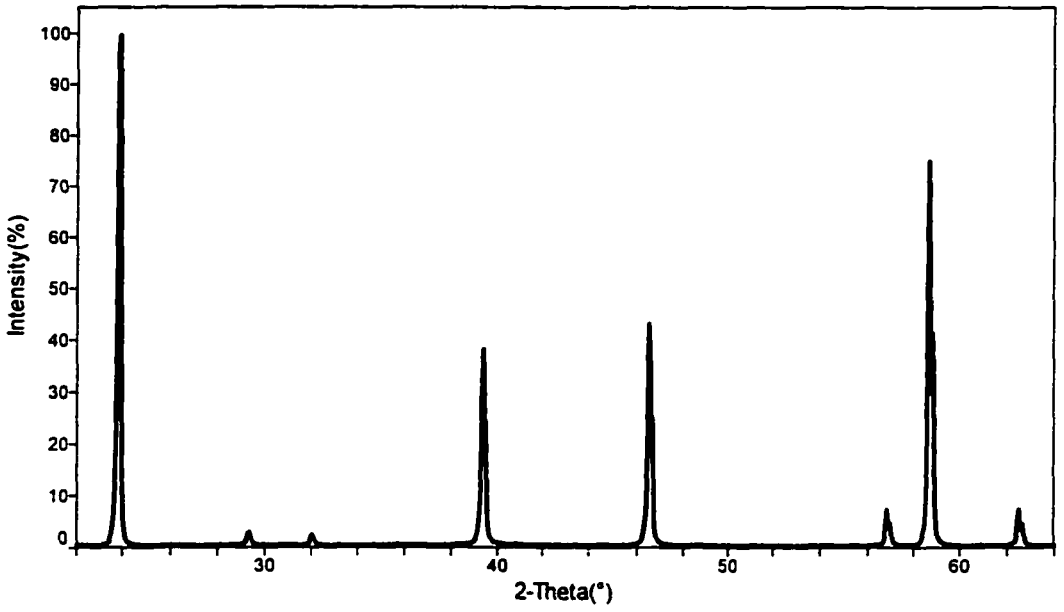

Figure 38: XRD of CdTe film deposited at 400°C at 12mTorr.

6.1.3 PL ANALYSIS.

Figure 39 shows the PL spectra of a typical CdTe film deposited at 380°C in 2mTorr pressure. Two curves are shown for 15K and 35K temperature measurements. No significant differences are observed from one bias to another at this pressure. However, films deposited with 12mTorr pressure had peak intensities considerably less than those of the 2mTorr films, as seen in Figure 40. This means that non-radiative recombination events are present in the 12mTorr films, indicating the presence of deep level defects. Also, there is significant variation of intensity with substrate bias at the higher pressure. Figure 41 shows the PL spectra at 15K for 12mTorr films deposited with 0V, –2V, and –12V substrate bias.

The increase in PL intensity with decreased pressure corresponds to increased grain definition observed in the SEM images. There is no significant change in PL intensity with bias at the lower pressure, which corresponds to no change in grain definition with bias (only in spacing.) However, the change in grain definition with bias is quite evident in the SEM images of the 12mTorr films, corresponding to the change PL intensity seen in Figure 41.

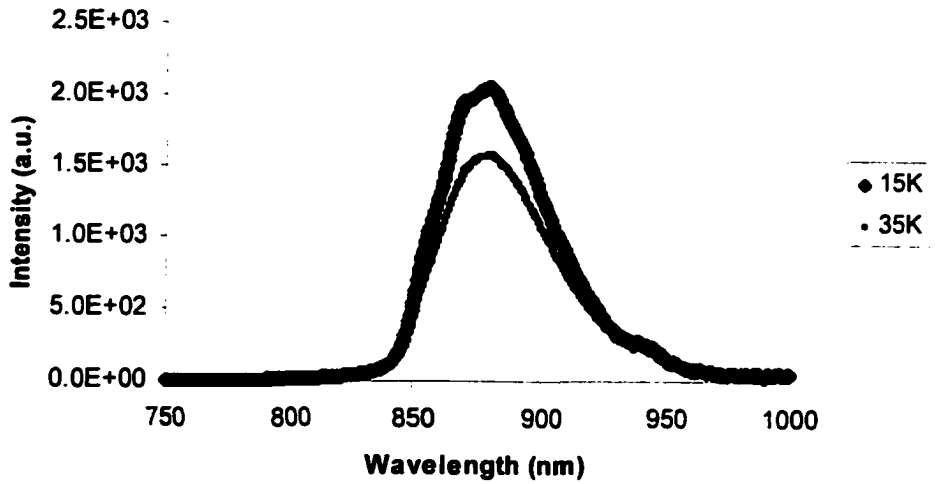

Figure 39: Typical PL of CdTe film deposited at 2mTorr.

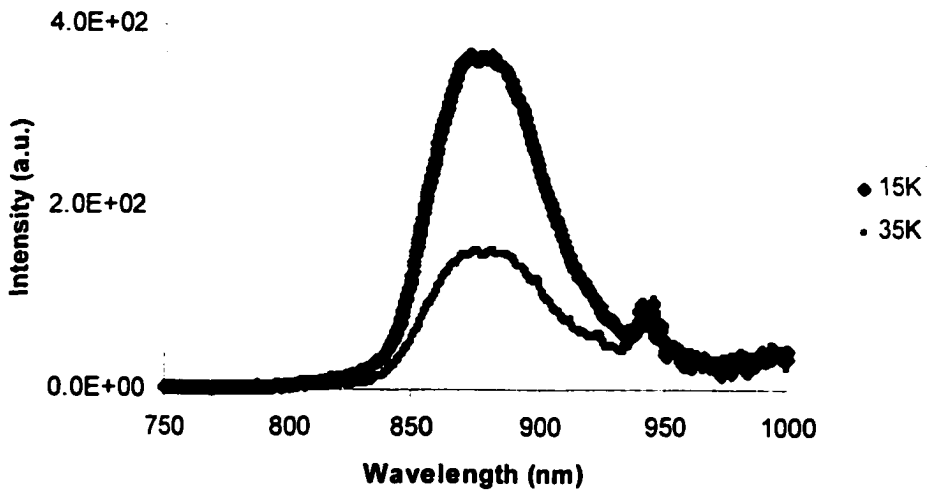

Figure 40: Typical PL of CdTe film deposited at 12mTorr.

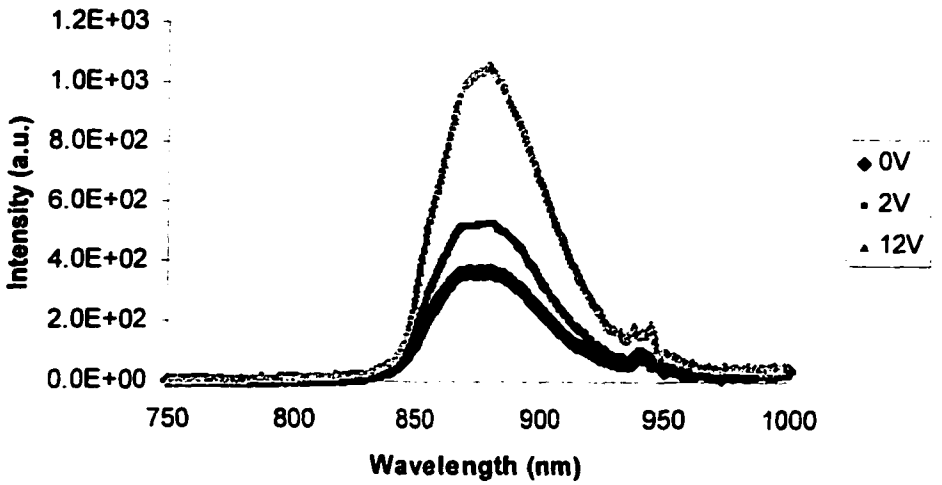

Figure 41: Relative PL intensities of CdTe films deposited with 0V, –2V, and –12V biases in 12mTorr.

6.1.4 DEVICE I-V ANALYSIS.

The original intent of this study was to fabricate CdS/CdTe solar cells with a substrate structure (described in Chapter 2, Figure 5), as opposed to the superstrate structure (described in Chapter 1, Figure 1), which is the focus of most of the research in CdTe-based solar cells. The intent was to use p^+-ZnTe as an interlayer (instead of Te and Cu) between the Mo substrate and the CdTe absorber layer to alleviate back contact problems. As will be explained in later sections, it turns out that this is not possible due to processing requirements. Singh[4], in fact, mentions attempting to use p-type ZnTe in his superstrate structures, but does not explain the reason for failure. However, comparison of some devices fabricated without a back-contact interlayer gives some confirmation of the film properties observed in the structural analysis.

Devices were fabricated by first depositing a 4μm CdTe film on a 0.1mm Mo foil substrate (which served as a back contact) at 380°C, 75W RF power, 2mTorr and 12mTorr pressure of pure Ar, and substrate biases of 0V, –2V, and –12V. After a standard $CdCl_2$ heat treatment, a 1μm film of In-doped n^+-CdS was deposited on the CdTe film in the simple RF diode sputtering mode, using 50W RF power, 5mTorr pressure, 350°C substrate temperature,

0V substrate bias, and 11cm target-substrate distance. The thickness of the films was necessary to prevent shorting. Contacts of 100Å of Cr (4mm diameter) were evaporated on the CdS, followed by a small dot of Ag paint on the Cr. The Cr contact has a transmission of about 30%. This should be considered when examining current magnitude.

Figure 42 shows current-voltage curves for the devices with 2mTorr CdTe films deposited at the various biases. Although the V_{oc} is severely limited due to the Schottky diode at the back contact, a few observations can be made to compare the various biases used to deposit the CdTe films. First, it is evident that V_{oc} decreases with heavy bias. Second, the −12V device appears to have shorted. Both of these phenomena are likely due to the fact that a heavy bias creates larger gaps in between grains. This can lead to lower V_{oc} because of the increase in grain-boundary defects. It is also seen that all devices have a low shunt resistance. This is likely caused by the roughness of the CdTe surface observed in the SEM images (Figures 16–18).

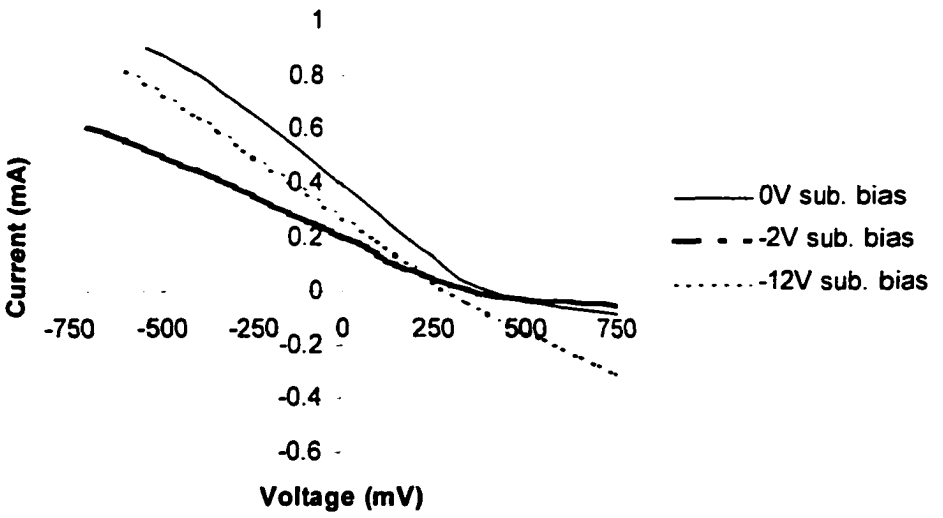

Figure 42: I-V curves for devices with CdTe layer deposited in 2mTorr at various substrate biases.

Figure 43 shows the current-voltage curve for a device with a 12mTorr CdTe layer at 0V. As can be seen, the V_{oc} of the device with the 12mTorr CdTe layer is significantly less

than that of the same device using a 2mTorr CdTe layer. Also, the I_{sc} is much less using a 12mTorr CdTe layer. These phenomena correlate to the difference in PL signal and grain definition seen with SEM. However, there is an improvement in shunt resistance over the 2mTorr device. This corresponds to the improvement in surface roughness with higher pressure as seen in the SEM images.

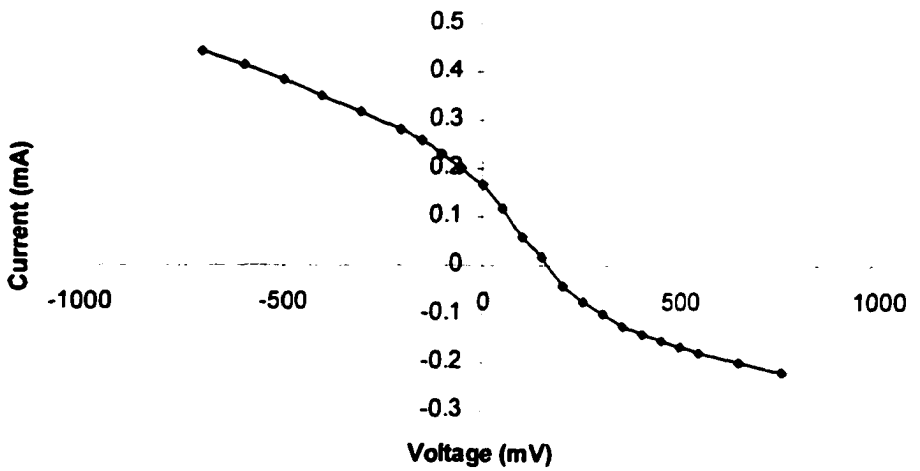

Figure 43: Typical I-V curve for device with CdTe layer deposited in 12mTorr.

6.1.5 REMARKS ABOUT TRIODE SPUTTERING CdTe

A few remarks are in order regarding triode sputtering of CdTe. First, triode sputtering enabled depositions at the low pressure of 2mTorr. It was not possible to sputter in the diode mode at pressures lower than 5mTorr with a stable plasma. This is likely due to the increased plasma density that triode sputtering offers, since the distance between electrodes is shortened (in this study, it was cut in half). Simply bringing the substrate closer to the target in diode mode would likely cause severe damage to the film, since the substrate would be immersed in the plasma. Triode sputtering actually takes away what plasma may have been reaching the substrate in diode mode. Ion bombardment of the substrate is then easily controlled with substrate bias. A side benefit is that the plasma is relatively unaffected by substrate bias. This enables better process control.

Because the grounded electrode is moved closer to the target electrode, an increase in the electric field results. Recall from Chapter 4 that the sputtering target, in diode mode, tends to erode in a ring, as in Figure 7. In this study, the CdTe target eroded in an inverse manner, as in Figure 44. This indicates a significant change in the electromagnetic field over the target which redirects the impact of sputtering ions.

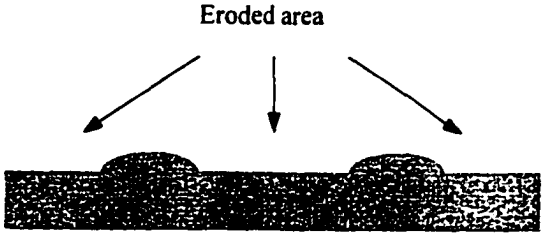

Figure 44: Cross section of CdTe target sputtered in triode mode.

6.2 Triode Sputtering of p^+-ZnTe Films.

Films of p-type ZnTe doped with N and Cu+N were deposited on Corning 7059 glass using triode sputtering. The substrate was positioned 6cm above the target, with the wire mesh positioned directly in between them. Except where otherwise noted, the substrate was heated to 425°C, the sputtering ambient was 5% N_2, and RF sputtering power was set at 75W. Deposition ambient pressure and substrate bias were varied. Again note that when bias is mentioned, it refers to substrate bias during deposition. After deposition some films were heated in air at various temperatures and times. Electronic properties of the films were analyzed with four-point probe and activation energy measurements. Raman measurements were performed for structural analysis.

6.2.1 THICKNESS.

This section of the study begins with films sputtered from at ZnTe target with 1% Cu. Figure 45 shows the thickness of films deposited at various substrate biases under 2mTorr ambient pressure. Film thickness was an average of 1.25μm with a deposition time of 1hr.

The thickness varied from deposition to deposition, as in any process. However, there was no correlation of thickness to bias. This is a very different result compared to CdTe films.

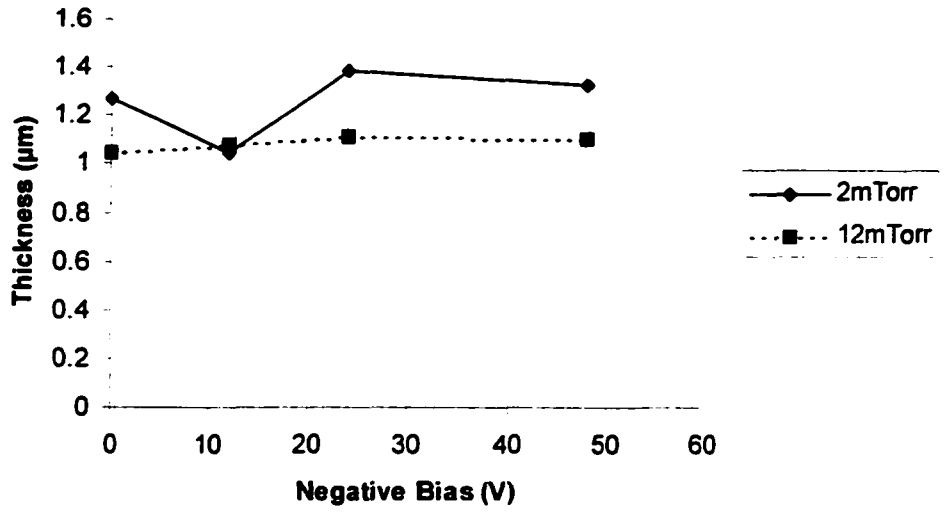

Figure 45: Thickness vs substrate bias of ZnTe films.

Figure 45 also shows the thickness of films deposited under 12mTorr pressure for 1hr. Again, there is no apparent correlation of thickness with bias. However, it is fairly clear that the increase in pressure leads to a decrease in film thickness, averaging 1.08µm. Also, the thickness variation from film to film was much less. That is, thickness was more consistent at the higher pressure.

Films sputtered from a pure ZnTe target exhibited the same lack of thickness variation as those sputtered from targets with 1%Cu. However, the average thickness of films deposited under 12mTorr pressure for 1hr was 1.21µm.

6.2.2 CONDUCTIVITY AND ACTIVATION ENERGY.

Figures 46 and 47 show the conductivity variation with bias of films sputtered from the 1%Cu target. At 2mTorr deposition pressure, conductivity was greater with an applied substrate bias than when the substrate was held at ground. This is a repeatable result.

However, the change in conductivity with various applied biases (–12V, –24V, and –48V) is likely due to process variation, as this result was not repeatable.

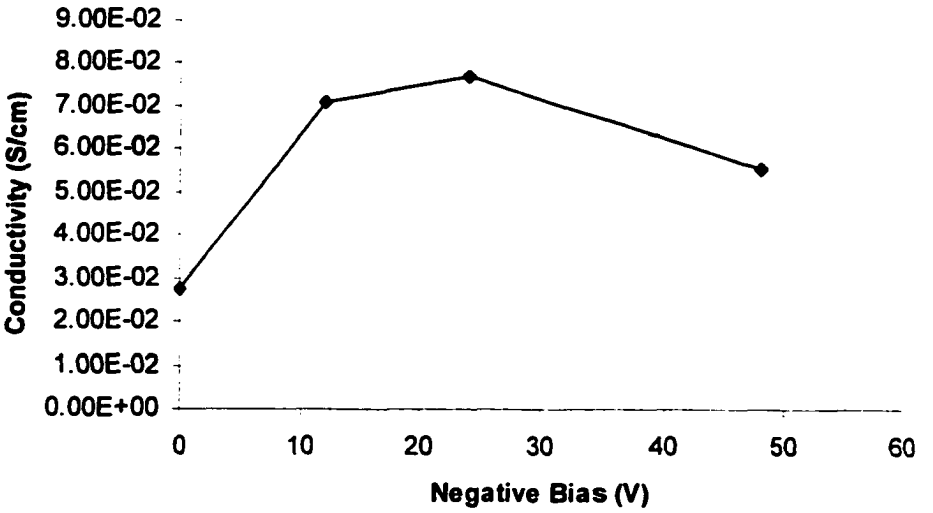

Figure 46: Conductivity vs. substrate bias for ZnTe films deposited from 1% Cu target at 2mTorr.

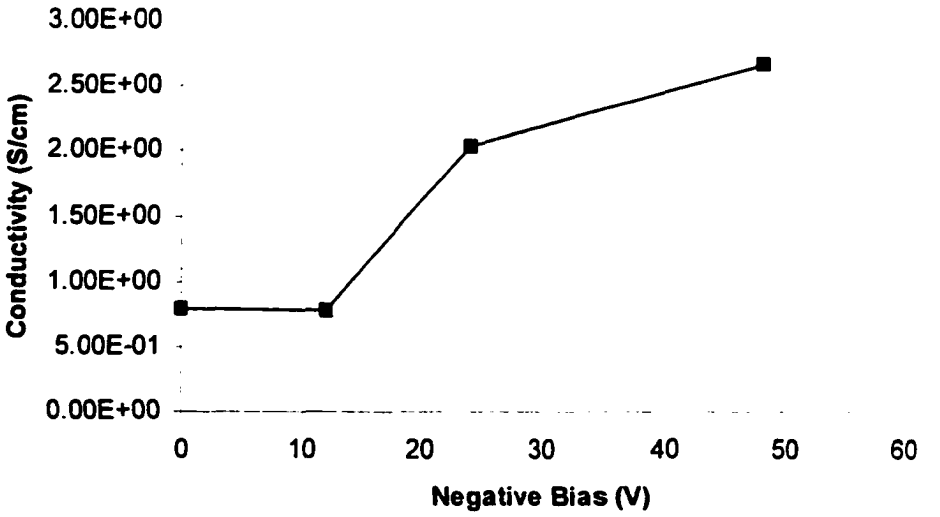

Figure 47: Conductivity vs. substrate bias for ZnTe films deposited from 1% Cu target at 12mTorr.

At 12mTorr deposition pressure, the same behavior in conductivity is seen with respect to bias variation, except that a larger bias is needed to significantly increase the conductivity. The most striking result, however, is the dramatic increase in conductivity with the higher pressure. This is apparently due to the increase in available N atoms for incorporation into the film for doping. Here, it is seen that an increase in deposition pressure from 2mTorr to 12mTorr leads to a factor of ~36 increase in conductivity from 0.08S/cm to 2.67S/cm. This can be compared to (diode sputtered) N-doped ZnTe films from Compaan,[19] which have a maximum conductivity of 0.1S/cm. This is not a direct comparison, however, since Compaan used a pure ZnTe target, and not one with 1%Cu.

Activation energy measurements showed a similar lack of correlation with bias, as well as a strong correlation with pressure. Figure 48 shows an example of a natural log plot of current vs. 1/kT.

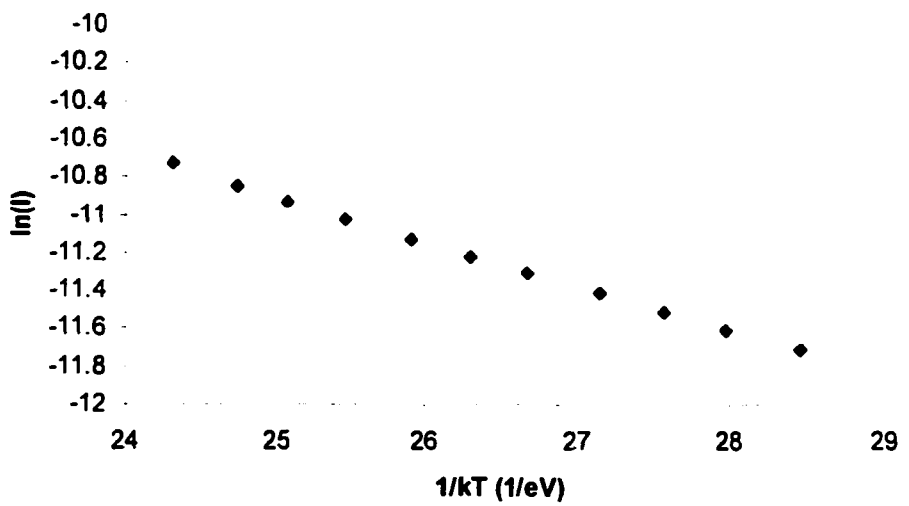

Figure 48: Activation energy measurement of a ZnTe film deposited from a 1%Cu target at 2mTorr. E_a=231meV.

At 2mTorr, activation energy was in the range of 200meV to 235meV, while at 12mTorr the activation energy decreases to a range of 125meV to 145meV. This decrease in activation energy with increased pressure corresponds to an increase in conductivity. This is to be expected, since the activation energy measurement for polycrystalline material is a

measurement of the barrier height at the grain boundaries, and the ability of carriers to surmount the barriers.

Films sputtered from a pure ZnTe target at 2mTorr had conductivities too low to measure with a four-point probe. Van der Pauw measurements gave readings on the order of 10^{-4}S/cm, although extensive measurements were not performed on the 2mTorr films. At 12mTorr, ZnTe films with thicknesses of ~1.2μm (1hr deposition time) had conductivities anywhere from 0.08S/cm to 0.21S/cm. This can be directly compared to Compaan's 0.1S/cm films. There was no correlation of conductivity to substrate bias in films of this thickness. Multiple films deposited with the same bias show this same spread in conductivity at this thickness.

As with the 1%Cu target, the activation energy of films deposited from the pure ZnTe target correlated well with conductivity. That is, higher conductivity corresponded with lower activation energy. As with conductivity, bias had no consistent effect on activation energy for films of this thickness. For 12mTorr films, activation energy was found to be between 100meV and 120meV. This is an improvement over films sputtered from the 1%Cu target. An example of the activation energy measurement for a film deposited at 12mTorr is given in Figure 49.

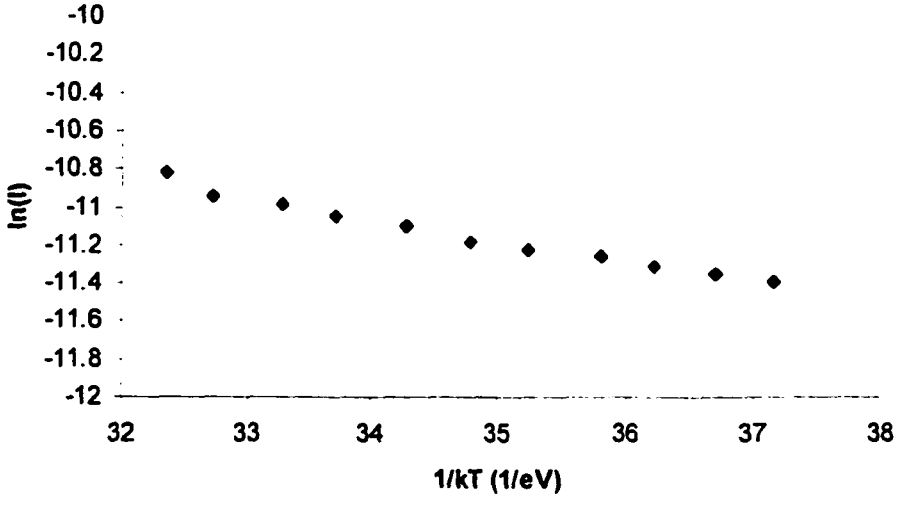

Figure 49: Activation energy measurement of a ZnTe film deposited from a pure target at 12mTorr. E_a=103meV.

Films with a thickness of ~0.6μm (0.5hr deposition), however, exhibited consistent, repeatable correlation of conductivity with substrate bias. Figure 50 shows conductivity vs. substrate bias of films deposited in 12mTorr pressure increasing from 0.09S/cm to 0.20S/cm when the bias is changed from 0V to –48V. These results indicate that Compaan, et al,[19] were correct when they suggested that ion bombardment might be affecting the films during deposition to increase conductivity. This is an interesting result in that a shorter deposition time (i.e., a smaller film thickness) yields more consistent film characteristics.

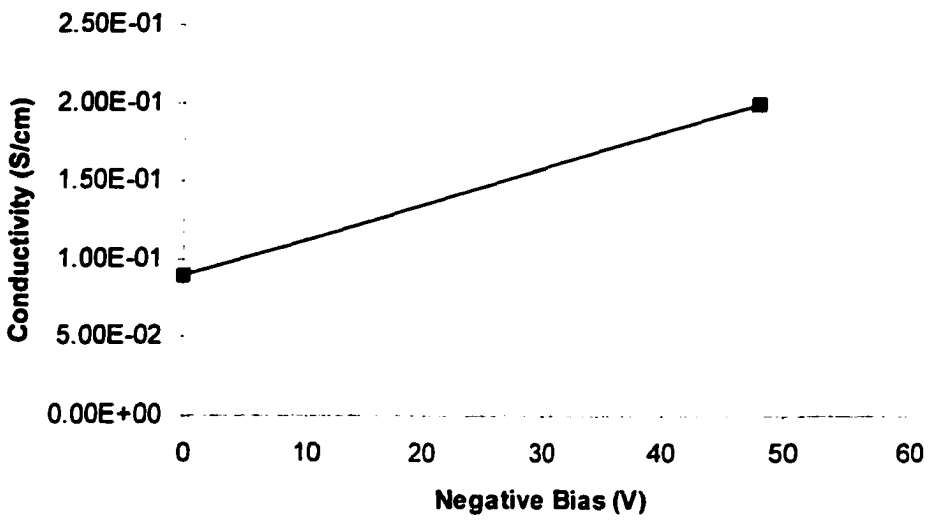

Figure 50: Conductivity vs. substrate bias for 0.6μm ZnTe films deposited from a pure ZnTe target at 12mTorr.

Activation energy, too, is found to change with substrate bias in a repeatable manner for films of this thickness, as shown in Figure 51. The difference in E_a for 0V and –48V is only 12meV, however. This corresponds to the aforementioned increase in conductivity. The values measured for activation energy are on the same order as, although slightly greater than, those of Compaan's lowest activation energy, 90meV.[13] The decrease in activation energy corresponds to the increased ion bombardment of the substrate that the bias induces. Ion bombardment would increase the surface velocity of the depositing material, creating a more structured film. Also, the ion bombardment would provide some etching of the film

during deposition, again creating a more ordered lattice. This, then, leads to the decrease in activation energy.

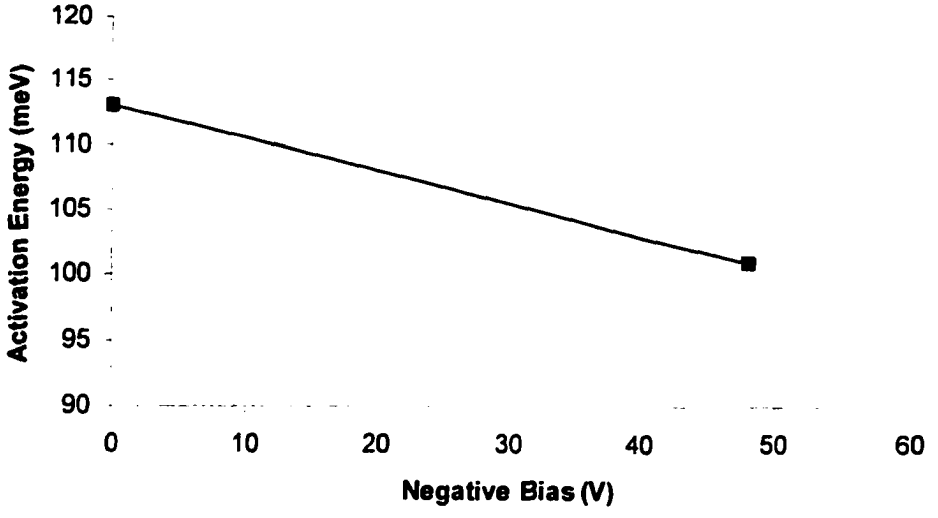

Figure 51: Activation energy vs. substrate bias for 0.6μm ZnTe films deposited from a pure ZnTe target at 12mTorr.

6.2.3 EFFECTS OF POST-DEPOSITION ANNEAL.

Films deposited from a pure ZnTe target with a substrate bias of –48V and a 5%N_2/95%Ar pressure of 12mTorr were annealed at various temperatures and times in air. As was seen with the effects of bias, annealing temperatures and times affected thicker (~1.2μm) films differently than thinner (~0.6μm) films.

The conductivity was measured at room temperature after deposition. The film was then annealed for 2hr and cooled to room temperature for another measurement. This cycle was repeated several times. Thickness was measured again as a precaution. There was no significant change in thickness after annealing. Figure 52 shows the normalized conductivity of a 0.6μm film annealed at 150°C for 2hr increments. The conductivity values were normalized to the as-deposited conductivity (in this particular case, 0.11S/cm) for purposes of comparison with other films. The conductivity increases very quickly at first, increasing

by a factor of 2.15 with the initial 2hr anneal. With subsequent anneals, the conductivity begins to level off. After three 2hr anneals at 150°C, the conductivity increases by 2.6.

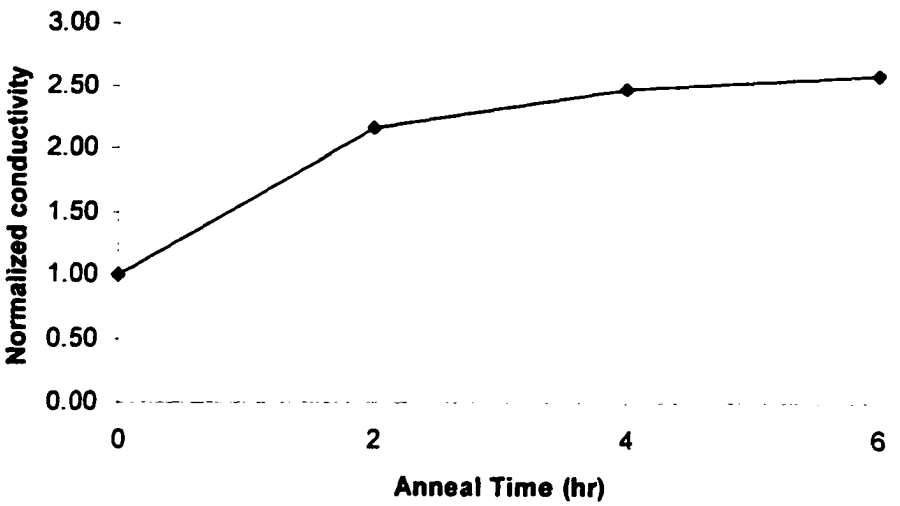

Figure 52: Conductivity vs. anneal time at 150°C normalized to as-deposited conductivity.

Figure 53 shows the normalized conductivity of films annealed for 2hr at 150°C, 250°C, and 350°C. The values shown are normalized to each film's as-deposited conductivity. The 150°C film was discussed above. Annealing at 250°C for 2hr or more did not increase the conductivity of the film. If there was any change in conductivity, it was a very slight decrease, but not significant enough to be outside the range of error. Finally, annealing at 350°C actually decreased the conductivity to just over a tenth of its as-deposited value. This explains why the use of a p^+-ZnTe layer in a solar cell with a substrate configuration (attempted in this study and by Singh[4]) failed. Since the ZnTe layer is deposited first, it is subjected to long periods of heat (>400°C) later in the processing when the CdTe and CdS layers are deposited and annealed. When this happened, the ZnTe layer was no longer conductive enough to allow tunneling through the barrier. Also, the series resistance of the device was likely increased because of the decrease in the ZnTe conductivity.

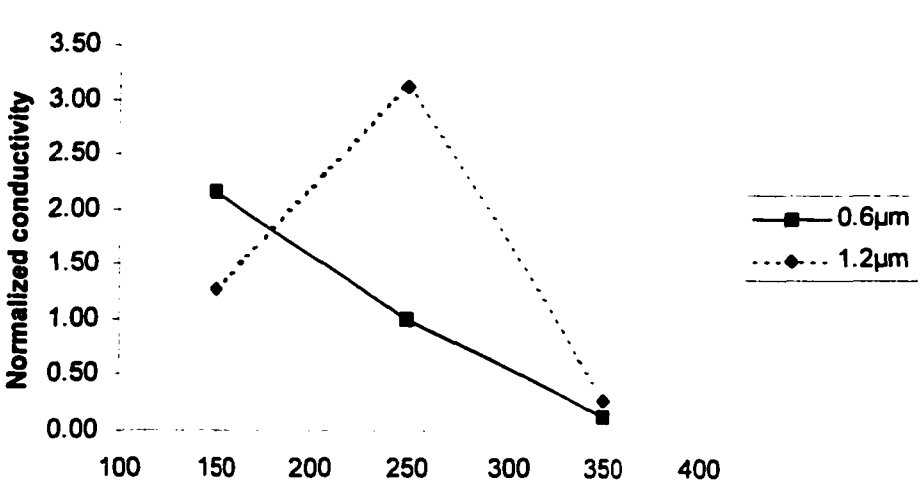

Figure 53: Normalized conductivity of ZnTe films annealed for 2hr at various temperatures.

Films of ~1.2μm thickness were deposited in the same manner as the 0.6μm films above. Figure 53 shows normalized conductivity of films annealed at various temperatures for 2hr. For these thicker films, a 150°C anneal increases conductivity by a factor of only 1.27, compared to 2.15 for the 0.6μm films. A 250°C anneal increases conductivity by more than a factor of 3, compared to no change for the 0.6μm films. Finally, the 350°C anneal decreases the conductivity by a factor of 0.28, compared to 0.12 for the 0.6μm films.

Here it is seen, therefore, that thicker films withstand and respond to higher anneal temperatures better than thinner films. Also, this suggests that there is an optimal anneal temperature for a given film thickness. In practice, a very thin (~0.1μm) ZnTe film is used at the back contact of a CdS/CdTe solar cell. A film of thickness 0.22μm was annealed at 150°C for 2hr. The conductivity was found to increase from an as-deposited value of 0.11S/cm to 0.26S/cm, a factor of 2.36. This is an even greater increase than that of the 0.6μm film.

Figure 54 shows the activation energy measured for the ~1.2μm films after a 2hr anneal at the various temperatures. For comparison, the activation energy for an unannealed film is included at 25°C on the graph. Since a combination of high temperature and small

thickness affects the electronic properties of the films, it was necessary to use the thicker films for this measurement, at temperatures in the range of 50°C to 90°C. Here it is seen that annealing the film increases the activation energy, which is counter to the fact that conductivity increases with annealing at 150°C and 250°C. An increase in activation energy indicates an increase in the energy barriers at the grain boundaries, which decreases conductivity. This would indicate that annealing at the appropriate temperatures has the effect of freeing carriers into a conductive state. This effect was also seen by Mochizuki[20] on epitaxial N-doped ZnTe films. In that study, however, higher annealing temperatures continued to increase the conductivity. For the polycrystalline films in this study, if the temperature is too high (e.g., ≥350°C), the effects might be too damaging to the film, or the film's structure may be changed in some way as to hinder conductivity.

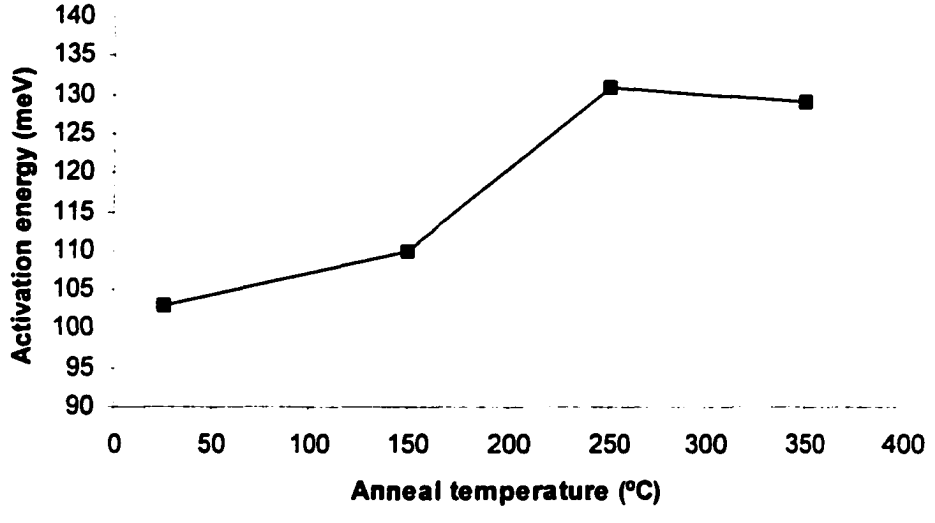

Figure 54: Activation energy of ZnTe films annealed for 2hr at various temperatures.

Raman measurements were performed on a number of the films in this study at the University of Toledo by A. Gupta. Figure 55 shows the Raman spectra for 1.2μm films annealed for 2hrs at the various temperatures. A comparison with Compaan[17] indicates that the film heated at 350°C may have a deficiency in N compared to the other films. This is

evident from the spike at 200cm^{-1}. Similar behavior is found in 0.6μm films. The N deficiency correlates to the significant decrease in conductivity of the 350°C annealed films.

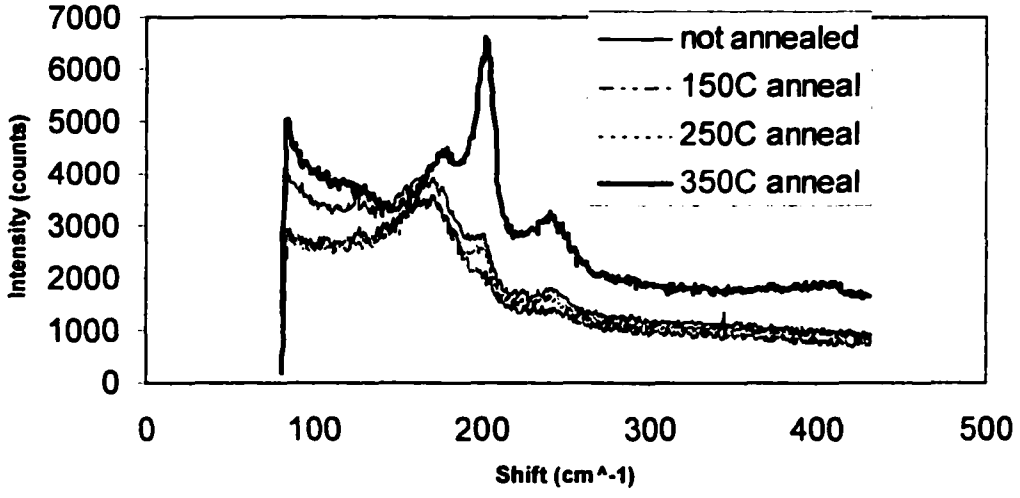

Figure 55: Raman spectra of 1.2μm films annealed 2hr at various temperatures.

6.3 N-Doped ZnTe Films in CdS/CdTe Solar Cells.

The final goal of this study is to use triode-sputtered N-doped ZnTe as the back contact layer to a CdS/CdTe solar cell and achieve reasonable and stable I-V characteristics. This section will show the results of that effort for a ZnTe interlayer sputtered on devices created here at the Microelectronics Research Center (MRC) and at the University of Toledo (UT). It will be shown that triode-sputtered N-doped ZnTe is indeed a viable option for a back contact layer of a CdS/CdTe superstrate solar cell. Also, various contacting schemes will be explored with respect to the metals used and annealing procedures.

6.3.1 VIABILITY OF TRIODE-SPUTTERED ZnTe FOR CdS/CdTe SOLAR CELLS.

Uncontacted solar cells were deposited similarly to reference 15 using diode sputtering at UT. The CdS and CdTe layers were 130nm and 2.4μm thick, respectively. A

$CdCl_2$ treatment was performed for 30min in air. Triode-sputtered N-doped ZnTe was deposited (here at the MRC) on the uncontacted solar cells immediately after a Br-methanol dip. Metal contacts, consisting of 150Å Te followed by 150Å Ni, were then evaporated. The contacts were circular with a 4mm diameter.

Using diode sputtering, Compaan[19] found that results were best when a 30nm intrinsic ZnTe layer was first deposited, followed by an 80nm N-doped layer. In this paper, this configuration will be referenced as a 'two-layer configuration.' It will be observed later that a single N-doped ZnTe layer of 2000Å (hereafter referenced as a 'one-layer configuration') yields lower V_{oc}. The two-layer configuration of ZnTe layers was used at the MRC (using triode sputtering) on the devices from UT. The resulting I-V curve is shown in Figure 56. For comparison, an I-V curve for the same contact without ZnTe is also shown.

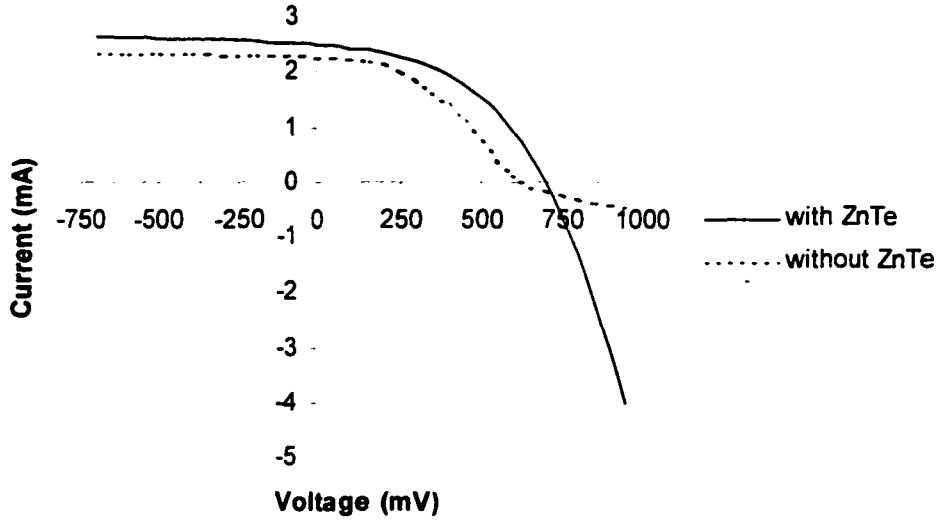

Figure 56: I-V curve of a device from UT with and without ZnTe at the back contact.

The device with ZnTe had a V_{oc} of 700mV and exhibited no 'roll-over' as seen in devices with poor back contacts (see Figure 3, as well as the non-ZnTe curve of Figure 56). These results are comparable to those of Compaan, who reports slight roll-over and V_{oc} of nearly 750mV.[19] Figures 57 and 58 show the relative QE spectrum and the QE ratio,

respectively, at 0V and 0.4V. (In this paper, unless otherwise stated, the phrase, "QE ratio," always refers to the ratio QE(V=0.4V)/QE(V=0V).) For comparison, Figure 58 also shows the QE ratio of the UT device without ZnTe at the back contact. The relative QE spectrum is typical for a CdS/CdTe solar cell.[21-23] The QE ratio shows that there are no particular collection problems at the CdS/CdTe junction or in the bulk of the CdTe layer. Comparison of the QE ratios for the same device with and without ZnTe at the back contact shows that the addition of ZnTe greatly improves the electric field of the device. The I-V and QE data show that triode-sputtered N-doped ZnTe is a viable option for use as a back contact to CdS/CdTe solar cells.

It should be noted at this point that annealing the devices at 150°C for 1-6hrs after contact deposition produced a slight degradation of solar cell performance. Typical I-V curves are shown in Figure 59 for as-deposited and annealed devices. There is a slight reduction in V_{oc} as well as an increase in series resistance. The QE spectra and QE ratios of annealed devices showed no noticeable change from those of as-deposited devices. The response of various contacting schemes to annealing will be explored in a later section using devices fabricated at the MRC.

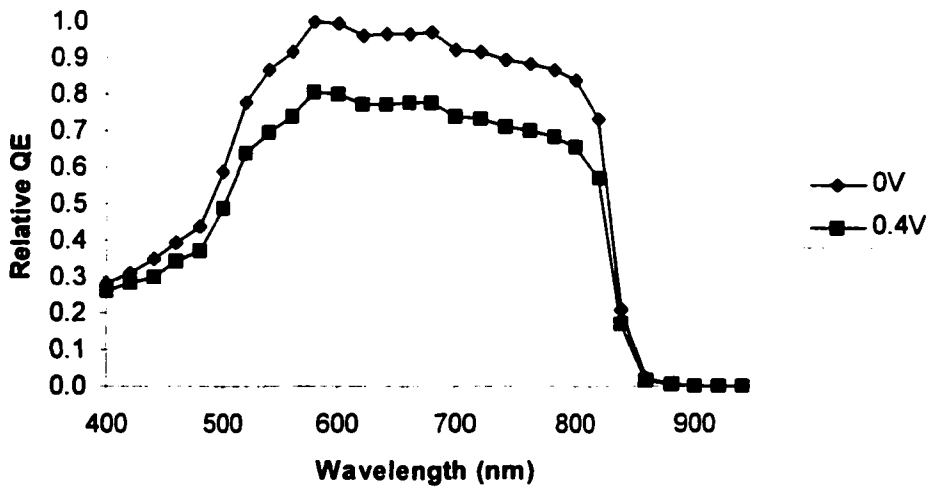

Figure 57: Relative QE of a device from UT with ZnTe at the back contact, at 0V and 0.4V.

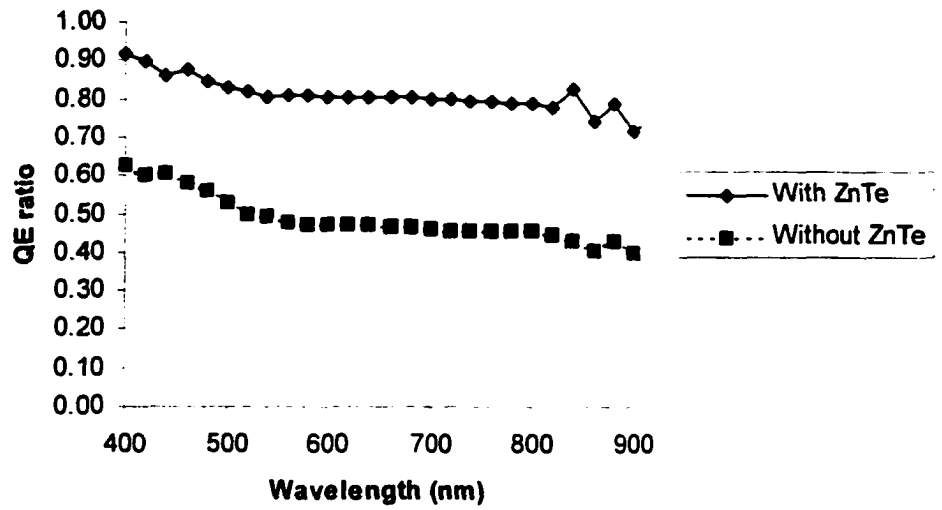

Figure 58: QE ratios of a device from UT with and without ZnTe at the back contact.

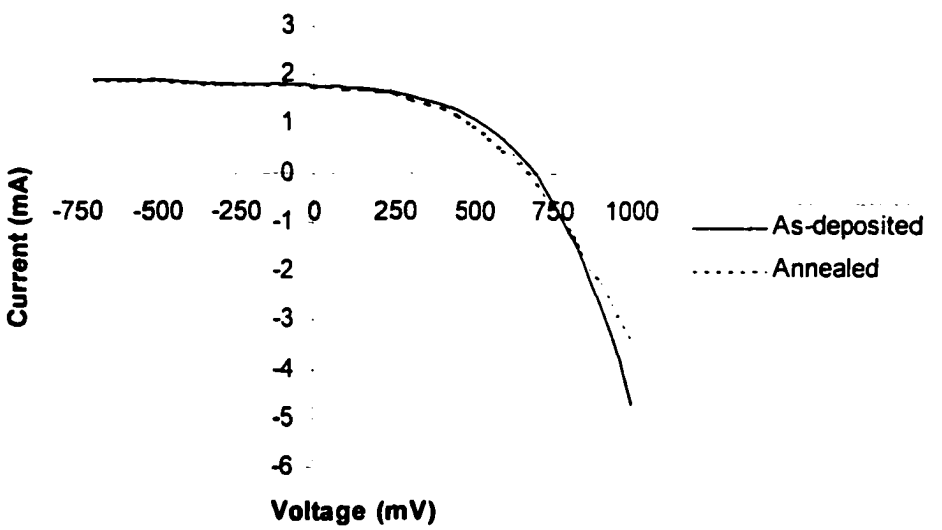

Figure 59: I-V curves of device from UT with ZnTe, as-deposited and annealed after contact deposition.

6.3.2 EFFECTS OF ANNEALING BEFORE CONTACTING

In light of the fact that the conductivity of N-doped ZnTe films (<0.7μm) increases significantly with annealing at 150°C, a device was fabricated by depositing contacts after annealing at 150°C for 1hr. Figure 60 shows the I-V curve of a device which was annealed in this manner before contact deposition, as well as that of a device not annealed before contacting. An improvement in V_{oc} is seen from 700mV to 720mV. The relative QE spectrum showed no changes from Figure 57. Also, the QE ratio showed no change from as-deposited devices.

The improved V_{oc} of devices annealed before contact deposition is in contrast to the fact that performance degrades slightly for devices annealed after contact deposition. The contact metal may be diffusing into the ZnTe and/or CdTe layers to create lattice defects which would inhibit current flow. This is not likely, however, since Te (diffusing from the Te/Ni contact) is a p-type dopant to ZnTe and CdTe, and should improve conductivity at the back contact.

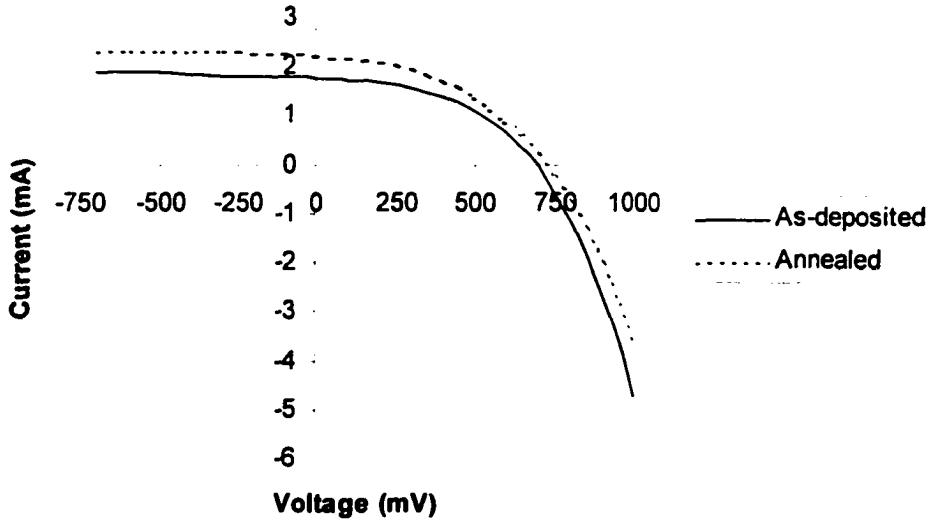

Figure 60: I-V curves of UT devices with ZnTe as-deposited and annealed before contact deposition.

6.3.3 EFFECTS OF VARIOUS CONTACT METALS.

CdS/CdTe devices fabricated at the MRC were deposited on SnO_2-coated soda-lime glass by the following procedure:

1. Clean substrate with ultrasonic bath of acetone followed by methanol.
2. Deposit ~1μm n^+-CdS by diode sputtering at 350°C, 5mTorr, 50W RF.
3. Perform $CdCl_2$ vapor anneal for 20min.
4. Deposit ~2.5μm CdTe by triode sputtering at 400°C, 15mTorr, 75W RF, 0V bias.
5. Perform $CdCl_2$ vapor anneal for 30min.

Devices were completed with 2000Å triode-sputtered N-doped ZnTe (one-layer configuration) using the same deposition parameters as for the devices from UT. Metals used for contacting were Ni and Pd. These metals were chosen for their high work functions which are needed to create a better contact to ZnTe. The performance of these various contacts will be examined with I-V and QE measurements.

For some contacts, the p-type dopants, Cu and Te, were deposited before Ni or Pd. It is known that the use of Cu, whether directly as a back-contact metal or as a dopant to ZnTe, creates an unstable back contact. It will be shown that this instability is exhibited in the QE ratio as the device is annealed, while the use of Te creates a slightly improved contact with respect to QE ratio.

The overall performance of the devices fabricated at the MRC was considerably less than the performance of the devices from UT. Although I_{sc} of MRC devices is in the same range as that of UT devices, V_{oc} is considerably lower in MRC devices, and a Schottky barrier is evident at the back contact. This is due to the differences in the CdS and CdTe layers. Clearly, more study is needed to improve fabrication of MRC devices. Despite the lesser overall performance of the MRC devices, comparison of the various metal contacts and annealing schemes for the same device is informative.

6.3.3.1 Comparison of Ni and Pd metal contacts.

Figures 61 and 62 show I-V curves of a device with Ni and Pd contacts, respectively. Each figure shows the progression of the I-V characteristics as the device is annealed at

150°C for 0, 3, and 7hrs. Initially, both contacts show the same I_{sc}, but the Ni contact shows a V_{oc} higher than that of the Pd contact by 50mV. Both contacts exhibited a small initial decrease in light current (I for V<0V) with annealing, and almost no change in V_{oc} over the 7hrs of total anneal time. As the device is further annealed, however, the Ni contact exhibits a decrease in fill factor from 0.34 after 3hrs of anneal, to 0.25 after 7hrs of anneal. The decrease in fill factor seems to be due to an increase in series resistance rather than a reduction in shunt resistance, since V_{oc} does not change The I-V curve of the Pd contact remains nearly constant, with a fill factor of 0.38.

The QE ratios for the Ni and Pd contacts are shown in Figure 63. The ratio is larger for the Ni contact than for the Pd contact. This corresponds to the larger V_{oc} of the Ni contact. The QE ratios for both contacts did not change significantly with annealing, which, again, corresponds to the unchanging V_{oc}. The combination of a decreasing fill factor and unchanging QE and V_{oc} for the Ni contact means that the contact itself is probably degrading and not disturbing the CdS/CdTe junction. It may be that Ni is simply diffusing away from the contact, thus increasing the contact resistance. A possible reason that the Pd contact is not degrading is that Pd is a larger atom than Ni, and hence, less mobile.

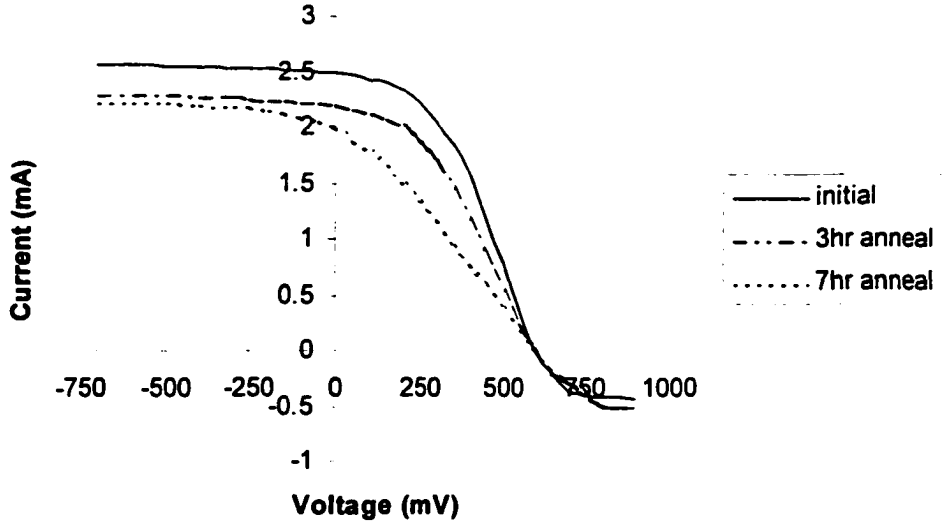

Figure 61: I-V curves of MRC device with Ni contact after various anneal times at 150°C.

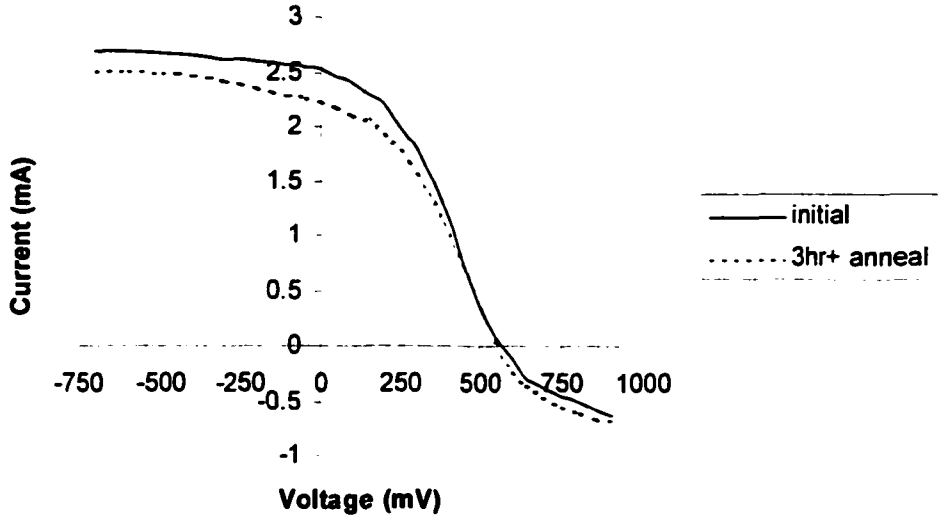

Figure 62: I-V curves of MRC device with Pd contact after various anneal times at 150°C.

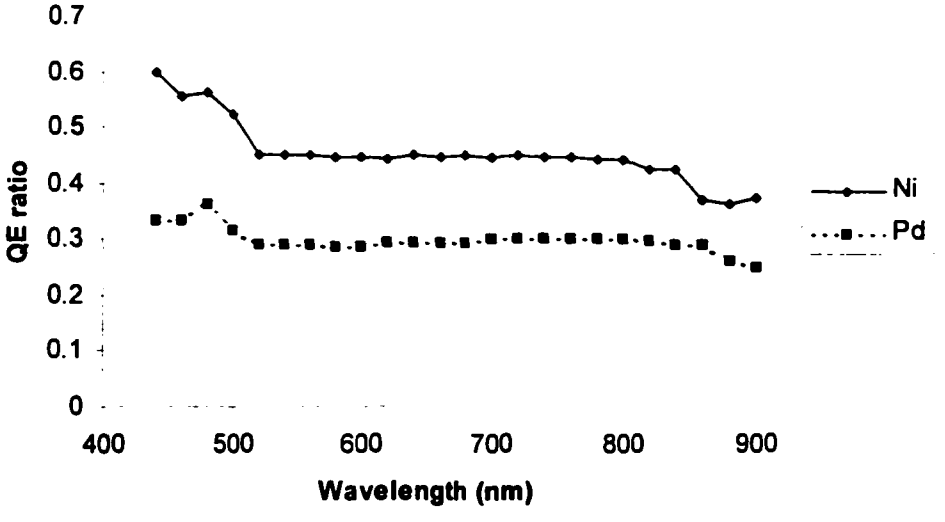

Figure 63: QE ratios of MRC device with Ni and Pd contacts.

6.3.3.2 Effects of the use of Cu in the contact.

For this subsection, 200Å of Cu was deposited before Ni or Pd. This was done on the same device as the Ni-only and Pd-only contacts. The I-V and QE characteristics were again examined as the device was annealed at 150°C for various times.

Figures 64 and 65 show the I-V curves of Cu/Ni and Cu/Pd contacts, respectively. Shown, again, is the progression of the I-V characteristics at successive anneal times. Initially, the contacts are extremely poor. After only 1hr anneal, both contacts show significant improvement. This behavior is to be expected, since Cu contacts typically require a sintering step.[10] The V_{oc}, I_{sc}, and fill factor of the Cu/Ni contact increase to 560mV, 2.2mA, and 0.47, respectively. Those of the Cu/Pd contact increase to 595mV, 2.6mA, and 0.45, respectively. Here it is seen that V_{oc} is larger for the Cu/Pd contact, and the Schottky barrier 'roll-over' is less pronounced. After 3hrs of annealing, the performance of the Cu/Ni contacts improves somewhat, while the I-V curve of the Cu/Pd contact remains the same. Further annealing thereafter results in degraded device performance for both contacts, with the Cu/Pd contact showing a more stable I-V curve than the Cu/Ni contact. This is similar to the comparison of contacts without Cu.

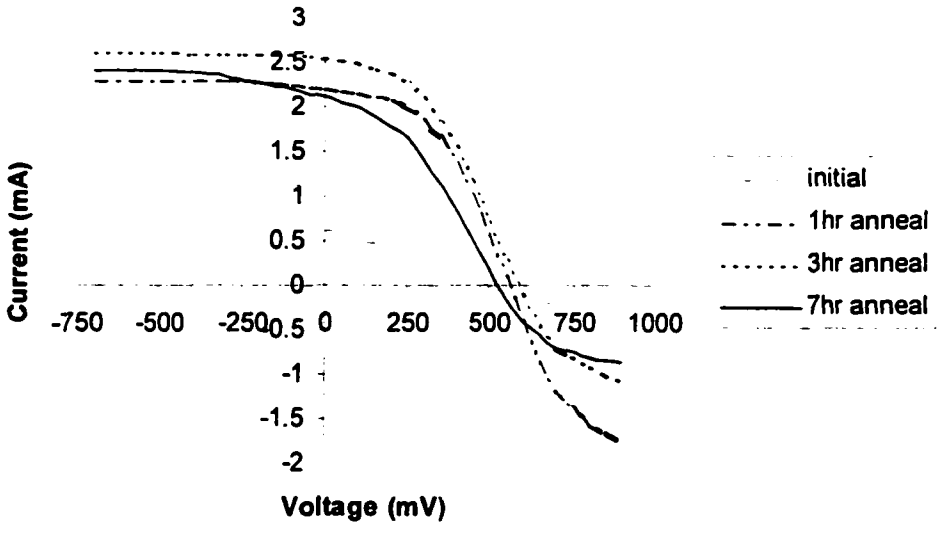

Figure 64: I-V curves of MRC device with Cu/Ni contact after various anneal times at 150°C.

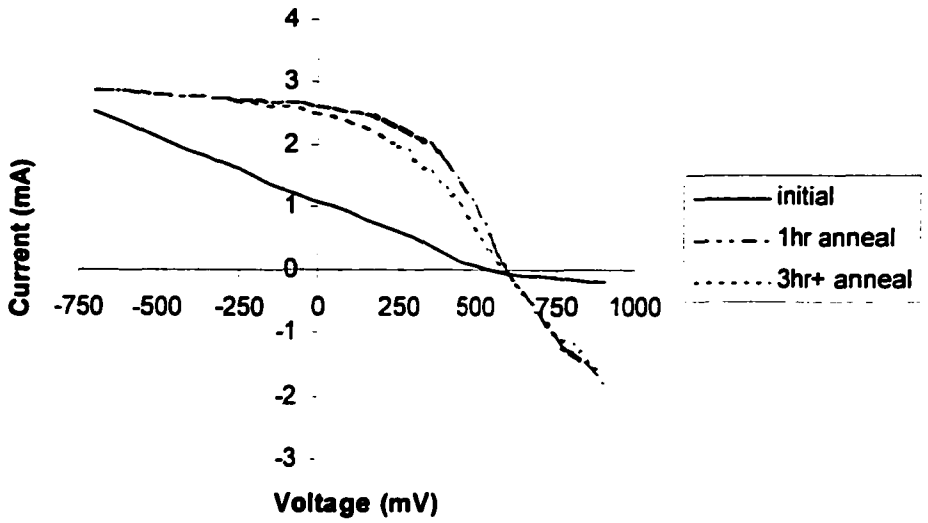

Figure 65: I-V curves of MRC device with Cu/Pd contact after various anneal times at 150°C.

The QE ratios for each contact show significant changes with annealing. Figure 66 shows the progression of the QE ratios with annealing times for the Cu/Ni contact. The initial QE ratio is extremely small, corresponding to the poor as-deposited I-V curve. After the initial 1hr anneal, the QE ratio approaches 0.9. This initial increase, again, is explained by the need for an initial Cu contact sintering. The QE ratio of the Cu/Ni contact is much larger than that of the Ni-only and Pd-only contacts. However, after 5hrs or more of annealing, the QE ratio decreases down to 0.6. Similar QE ratio characteristics are seen with the Cu/Pd contact.

The changing QE ratio with annealing is not seen with Ni-only and Pd-only contacts. This indicates that the Cu is mobile enough to diffuse all the way to the CdS/CdTe junction to create defects and degrade the electric field there. Another possibility is that, as the Cu diffuses away from the back contact, it increases the Schottky barrier. This also has the effect of reducing the internal electric field at the junction. It is well known that the I-V performance of CdS/CdTe devices using Cu at the back contact degrades (in the form of decreased V_{oc} and increased series resistance) with prolonged exposure to temperatures

>100°C.[24] However, it is believed that this is the first time a decrease in QE ratio has been shown.

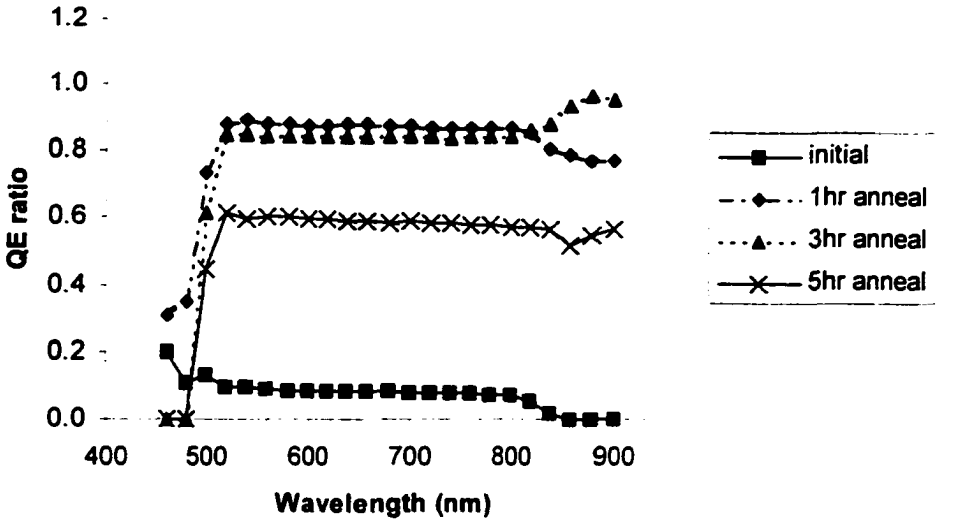

Figure 66: QE ratios of MRC device with Cu/Ni contact after various anneal times at 150°C.

6.3.3.3 Effects of the use of Te in the contact.

For this subsection, 200Å of Te were deposited before Ni or Pd. This was done on the same device as the Ni-only and Pd-only contacts. The I-V and QE characteristics were again examined as the device was annealed at 150°C for various times. The results for the Te/Ni are presented here. Nearly identical results were obtained for Te/Pd.

Figure 67 shows the I-V curves for the contact as-deposited and annealed for 3hrs. There was no change in the I-V characteristics after 5hrs and 7hrs of annealing. These results, compared to those of the Ni-only contact, show a significant improvement in the stability of the fill factor, but a small decrease in V_{oc}. The QE ratio of the Te/Ni contact is nearly identical to that of the Ni-only contact (see Figure 63) and did not change with annealing.

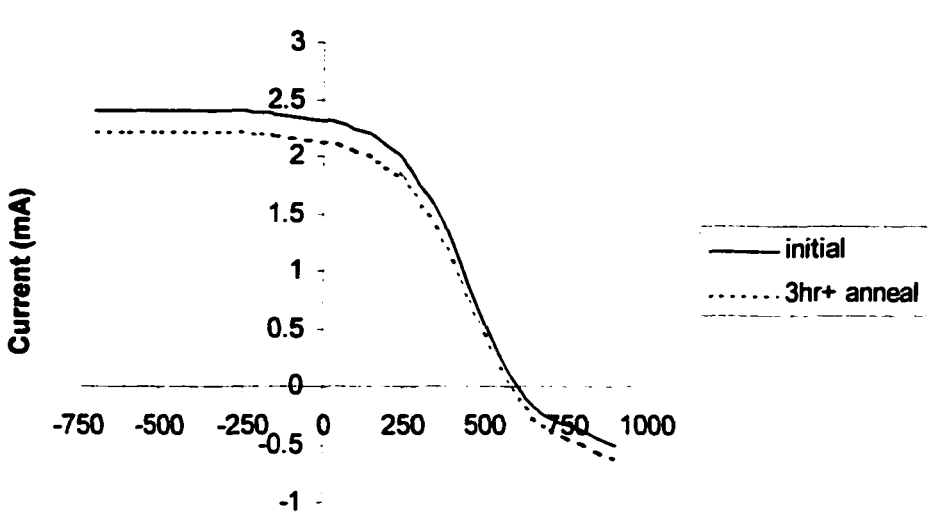

Figure 67: I-V curves of MRC device with Te/Ni contact after various anneal times at 150°C.

6.3.3.4 ZnTe/p^+-ZnTe (two-layer) configuration on MRC devices.

In 6.3.1 and 6.3.2, the ZnTe interlayer was of the two-layer configuration (previously described in 6.3.1). This configuration was used for devices from UT. In 6.3.3 so far, the configuration has been the one-layer configuration, and was used for MRC devices. In this subsection, the two-layer configuration will be applied to MRC devices using a Te/Ni contact. This will allow a direct comparison of the two ZnTe configurations.

Figure 68 shows the I-V curve of an as-deposited MRC device with the two-layer ZnTe configuration. A comparison with Figure 67 shows significant improvement in V_{oc} over a device with the one-layer configuration. Also, the Schottky barrier 'roll-over' is much less pronounced. An anneal of the device at 150°C for 2hr showed a slight decrease of the fill factor, which is similar to devices previously described.

The QE ratio of the MRC device with the two-layer ZnTe configuration is shown in Figure 69. A comparison with Figure 63 (and remembering the QE ratios of the Ni and Te/Ni contacts were nearly identical) shows an improvement over the one-layer configuration, which corresponds to the improved V_{oc}. The use of the two-layer

configuration, therefore, improves the internal electric field of the device and facilitates tunneling at the back contact. This reduces the effect of the Schottky barrier on the device performance.

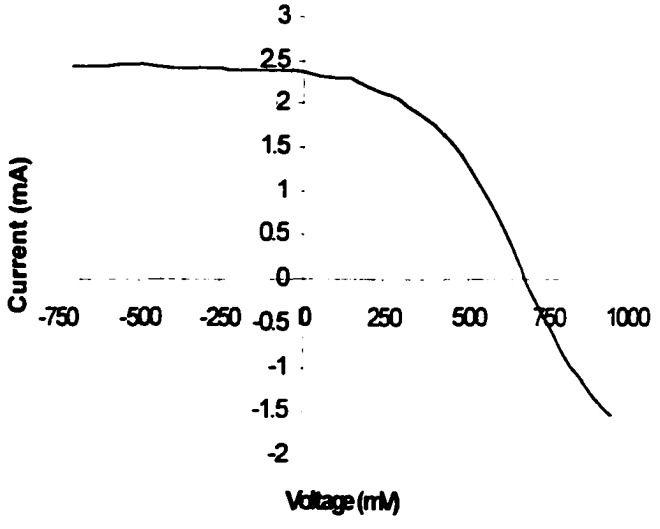

Figure 68: As-deposited I-V curve of MRC device with two-layer ZnTe configuration.

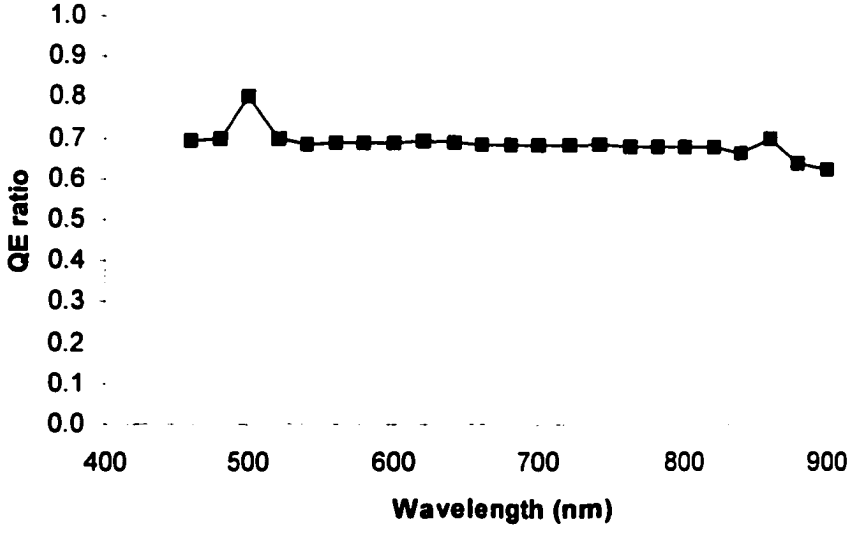

Figure 69: As-deposited QE ratio of MRC device with two-layer ZnTe configuration.

CHAPTER 7: CONCLUSIONS

This dissertation focused on the use of RF triode sputtering as a technique for deposition of thin-film solar cells. This is the first known study to make use of this technique for deposition of semiconductor material. To date, it has only been used for metals using DC power. Specifically, triode sputtering was used to deposit CdTe and ZnTe films. Films of CdTe were found to have well-defined grains when deposited under a low pressure (2mTorr) ambient, while grains were not as well defined when films were deposited under a higher pressure (12mTorr) ambient. Films deposited under low pressure showed little structural dependence on substrate bias. At higher pressure, a substrate bias of –12V produced films with more grain definition than films deposited with 0V or –2V substrate bias. Larger substrate bias has the effect of etching the film during deposition. XRD analysis indicates that increasing substrate temperature or bias produces films with random grain orientation. The films with well-defined grains exhibit a much larger PL intensity. This is an indication of fewer defect states near midgap. Films deposited at lower pressures, for example, exhibit PL intensity near an order of magnitude higher than films deposited at higher pressures.

N-doped ZnTe films were deposited using the triode sputtering technique. Films deposited using a 1%Cu/ZnTe target exhibited conductivities of 2.6S/cm or more when deposited under a higher (12mTorr) pressure and bias (–24V– –48V). For low pressure deposition, the conductivity was an order of magnitude smaller than for higher pressure films. Films deposited using a pure ZnTe target exhibited conductivities of 0.15S/cm or more under higher pressure and larger bias, with activation energies in the range of 100meV to 120meV. Conductivity of thinner (~0.6μm) films exhibited a consistent dependence on substrate bias, increasing with stronger bias. Activation energy decreased with stronger substrate bias. The conductivity and activation energy of thicker (~1.2μm) films showed no consistent dependence on substrate bias.

The effects of a post deposition anneal were studied on N-doped ZnTe films deposited from a pure ZnTe target under 12mTorr pressure and –48V bias. It was found that annealing a 0.6μm film for 2hr at 150°C results in conductivity increasing by more than a factor of 2.5. For a 250°C anneal, the conductivity is nearly unchanged, and for a 350°C

anneal, the conductivity decreases to ~12% of the initial value. In all cases, the activation energy is found to increase, indicating an increase in energy barriers at the grain boundaries. This means that carriers are somehow freed into a conductive state for the 150°C anneal. Raman measurements indicate that the films annealed at 350°C have a severe N deficiency, which explains the decrease in conductivity. It was further found that annealing 1.2μm films at 150°C results in an increase in conductivity by only 25%, while annealing at 250°C increases the conductivity by more than a factor of 3. Again, annealing at 350°C reduces the conductivity, but to a lesser extent than for the 0.6μm films. This indicates that there is an optimal temperature (and perhaps optimal time) for annealing a film of a given thickness. The fact that conductivity decreases severely with high anneal temperatures explains why efforts to fabricate a substrate structure with ZnTe at the back contact (the first layer deposited) have failed.

Triode-sputtered N-doped ZnTe was successfully used as an interlayer at the back contact of a device from the University of Toledo. A V_{oc} of 700mV was achieved. The I-V curve exhibited no Schottky barrier roll-over. Annealing the device after contact deposition resulted in a slight decrease in fill factor and a slight increase in series resistance. Annealing the device before contact deposition resulted in a 20mV increase in V_{oc}.

Finally, various contact metals and anneal procedures were studied on devices fabricated here at the Microelectronics Research Center. Pd and Ni were chosen as the primary contacts because of their high work functions. Ni was found to have a higher V_{oc} than Pd, but was not as stable with annealing at 150°C. The instability was exhibited in the degradation of the fill factor and increase in series resistance. Also, the QE ratio (QE(0.4V)/QE(0V)) was found to be smaller for the Pd contact. There was no significant change in QE ratio with annealing. Cu was then used in conjunction with Ni and Pd, with Cu being deposited first. An initial anneal step was necessary to create a good contact when Cu was used. After a 1hr anneal, V_{oc} of the Cu/Ni contact reached a peak, after which it began to decrease with more anneal time. The same is true for the QE ratio. This represents the degradation of a back contact when Cu is used. The QE ratio of the Cu/Pd contact also fell with increasing anneal time, but the V_{oc} did not continue to fall. Te was finally used in conjunction with Ni and Pd in the same way as Cu. For both Ni and Pd, the use of Te

resulted in increased stability (i.e. little change with annealing), although initial V_{oc} values were slightly less than for Ni-only and Pd-only contacts.

CHAPTER 8: SUGGESTIONS FOR FUTURE RESEARCH

The data on N doping of ZnTe are very interesting. They suggest that the activation of N dopant in polycrystalline films, and even the physical location of N within the films, may depend strongly on the preparation conditions and annealing. SIMS data to measure N content, and Hall measurements to measure mobilities and carrier concentrations should be done. Such measurements were attempted in this work, but only an estimate, within a factor of 2-3, of the mobility was possible because of the very large noise associated with small Hall signals for small mobility (<1 cm2/V-sec) materials. A new Hall system with rotating magnet or sample may have to be set up and the ac Hall voltage measured using Lock-In amplification techniques. If one can control the N doping of ZnTe accurately, and quantify it, then, it may be possible to solve the back contact problem for CdTe solar cells. This would be a major technical development. It was shown in this study that N doped ZnTe indeed helps to improve the back contact, and this further research may improve the contact beyond what was possible to do here.

Another area of interest may be the development of (Zn,Cd)Te system for graded bandgap solar cells.

APPENDIX: STANDARD OPERATING PROCEDURE FOR $CdCl_2$ VAPOR ANNEALING SYSTEM

1. Make sure valves on vacuum system are closed.

2. SLOWLY open N_2 valve. Monitor baretron readout to see when N_2 starts to enter tube. When reading is off scale, stop opening N_2 valve. Allow system to come to atmospheric pressure. Make sure cap on vacuum system does not pop off.

3. Close N_2 valve.

4. While holding glass end cap of furnace tube, carefully remove cap bracket.

5. Place glass end cap on table. Make sure glass rod is supported so that cap does not fall off of table.

6. Load sample into open-ended ampoule with tweezers. Sample should be almost to neck of ampoule.

7. Insert quartz wool into end of ampoule. The amount of wool should be just enough to close off the end of the ampoule. Make sure not to get many strands into the ampoule on the sample.

8. Make sure O-ring is clean, especially of quartz wool. Place O-ring in place and attach glass end cap back on furnace tube with bracket.

9. Turn on tube furnace and set to ~20°C above desired anneal temperature (set in °C). The furnace may have to be plugged in, as the power outlet is shared with the RF generator on the sputtering system.

10. Open the green vacuum valve to pump down the furnace tube.

11. When the baretron shows a reading, open the black vacuum valve and close the green valve.

12. Allow the tube to pump down as low as possible (takes 30 sec to 1 min). SLOWLY open N_2 valve (leave vacuum valve open) until pressure is off of baretron scale (>100 Torr). Close N_2 valve. This is a purge.

13. Repeat step 12 1-3 times.

14. When tube is pumped sufficiently, zero the baretron.

15. Open Ar and O_2 valves, in that order. Adjust flow controls to desired levels (if not already done.)

16. Close black vacuum valve. Allow pressure to rise near the desired level. Use green vacuum valve to adjust pressure.

17. Continue to let furnace rise to set temperature (with gases flowing). When all zones of furnace come to temperature, let sit for ~10 min.

18. Set temperature down to anneal temperature. Allow furnace to come down to temperature, then let sit for ~10 min.

19. Open push rod sealer and push ampoule into center of furnace. Make sure ampoule is in center of furnace. Closes push rod sealer. Leave ampoule in furnace for desired time.

20. Adjust pressure with green vacuum valve so that pressure is within ~0.3 Torr of desired pressure. Pressure will continually need adjustment during anneal.

21. At end of anneal time, turn furnace off, close O_2 valve, and close green vacuum valve, in that order.

22. SLOWLY open N_2 as in step 2 to bring furnace tube to atmospheric pressure. Close N_2 valve.

23. Open push rod seal. Pull ampoule out with push rod at slow rate (e.g., 1"/30 sec).

24. When ampoule is out of furnace, close push rod seal and open green vacuum valve.

25. When baretron has a reading, open black vacuum valve and close green valve.

26. Allow tube to pump down. Close black vacuum valve and allow ampoule to cool enough to handle with rubber gloves.

27. When ampoule is cool, remove glass end cap as in steps 1-5.

28. Remove quartz wool carefully and with rubber gloves so as not to make a mess.

29. Remove sample with tweezers.

30. Replace quartz wool or discard, depending on how much it has been used.

31. Replace glass end cap as in step 8.

32. Pump down furnace tube as in steps 10-11.

33. Close black vacuum valve and let sit.

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